



**Notes:**

1. FPGA Schematic Symbol Breakdown:
  - (a) Bank2 - IO
  - (b) Bank3 - IO
  - (c) Bank4 - IO
  - (d) Bank5 - IO
  - (e) Bank6 - IO
  - (f) Bank7 - IO
  - (g) Bank8 - IO
  - (h) Bank9 - IO
  - (i) Configuration
  - (j) Clocks
  - (k) VCCint, GND
  - (l) VCC0, GND

2. PCB Supports 2C70 - 2C50 - 2C70 Migration  
 No additional IO of 2C70 or 2C50 used as the 2C70 has the fewest IO of the group due to additional VCCINT, GND, and VREF pins on the larger 2C50 and 2C70 devices.

3. Some IO pins are connected to 1.2V and GND. These are the additional VCC and GND pins of the larger 2C50 and 2C70.

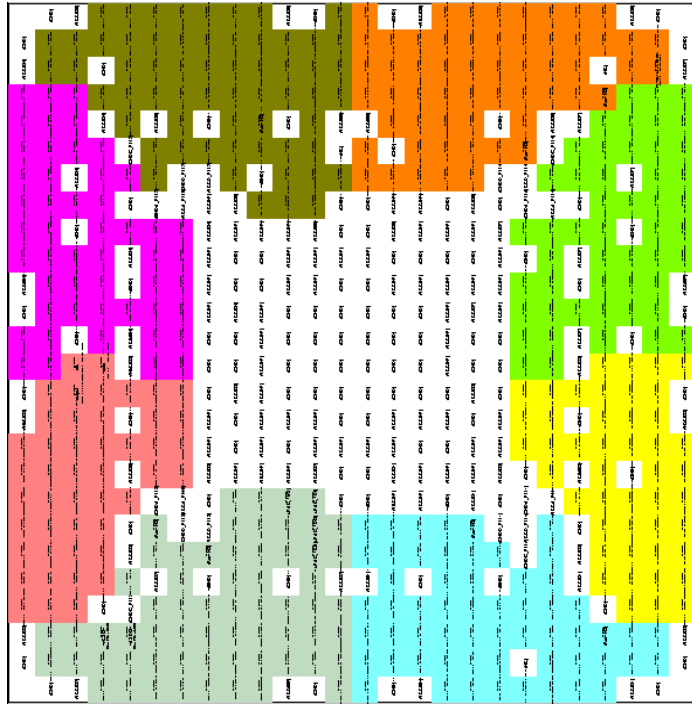
**--- WARNING ---**

**DO NOT DRIVE UNUSED IO TO GND IN QUARTUS**  
 Leaving 1.2V-connected IO pins as outputs driving GND causes high IO current and increased temperature which can lead to device damage if left over a long period of time.

**FPGA Package Top View  
 (2C70 Device Shown)**

**BANK 3**  
**VCCIO = 1.8V**  
 DDR2 DIMM DATA LANES  
 ADC Channel 2

**BANK 4**  
**VCCIO = 1.8V**  
 DDR2 DIMM DATA LANES  
 ADC Channel 1  
 ADC Channel 2



**BANK 2**  
**VCCIO = 3.3V**  
 Proto Bus  
 Video DAC  
 DAC Channel 1

**BANK 1**  
**VCCIO = 3.3V**  
 DAC Channel 1  
 DAC Channel 2  
 Video DAC

**BANK 5**  
**VCCIO = 3.3V**  
 Shared Bus  
 DAC Channel 2

**BANK 6**  
**VCCIO = 3.3V**  
 Shared Bus  
 DAC Channel 1  
 DAC Channel 2  
 Video DAC

**BANK 8**  
**VCCIO = 1.8V**  
 DDR2 DIMM DATA LANES, ADDRESS  
 Pushbuttons

**BANK 7**  
**VCCIO = 1.8V**  
 DDR2 DIMM DATA LANES, CNTL, CLOCK  
 Pushbuttons  
 Dipswitch



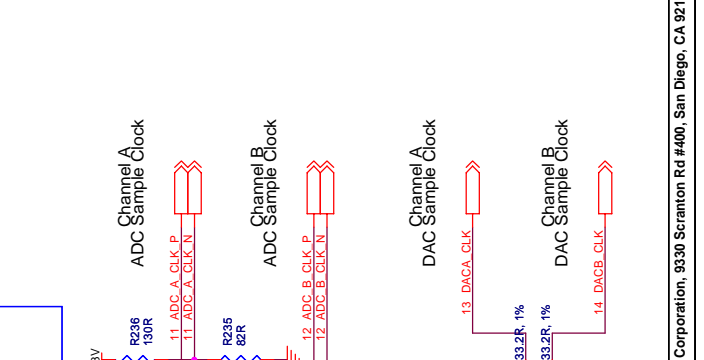
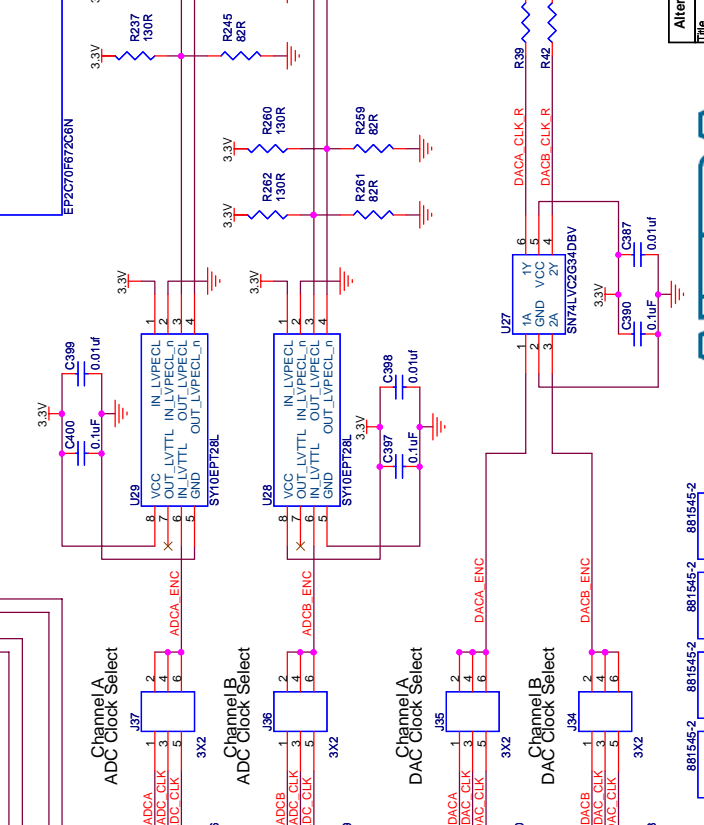
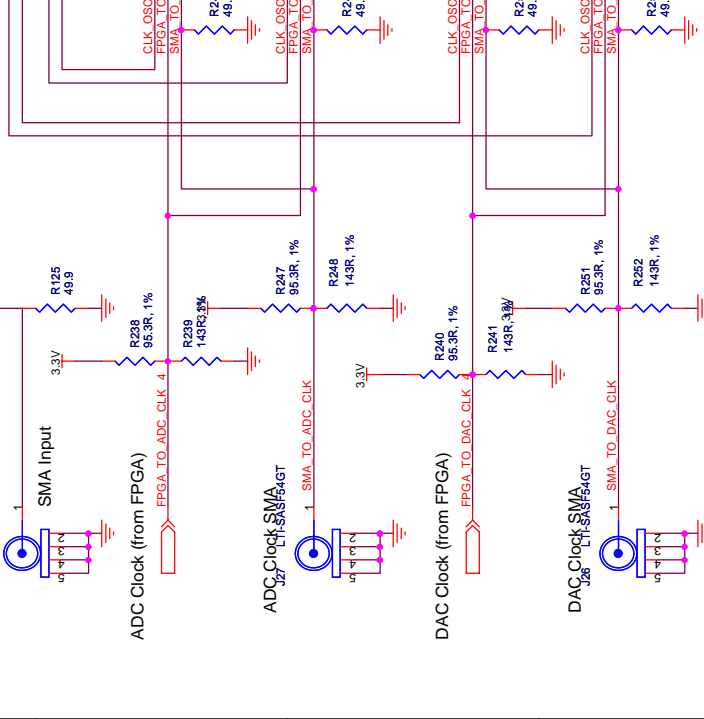
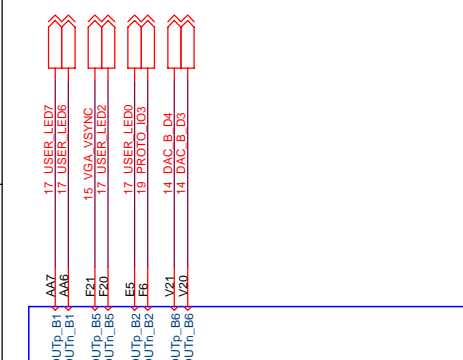
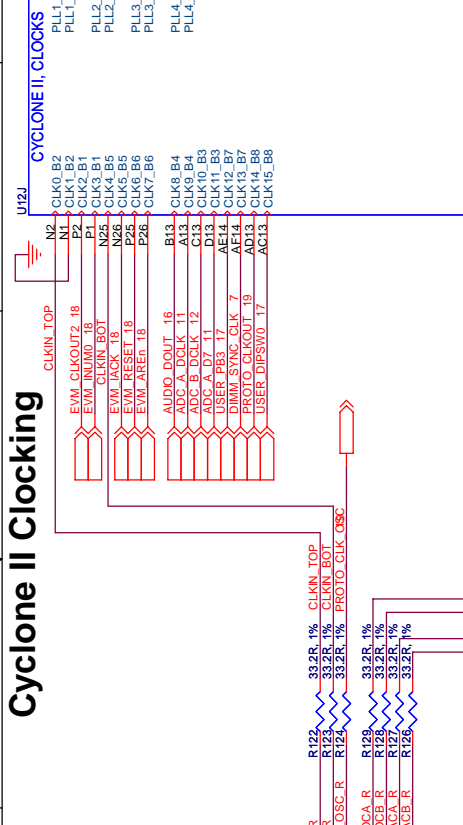
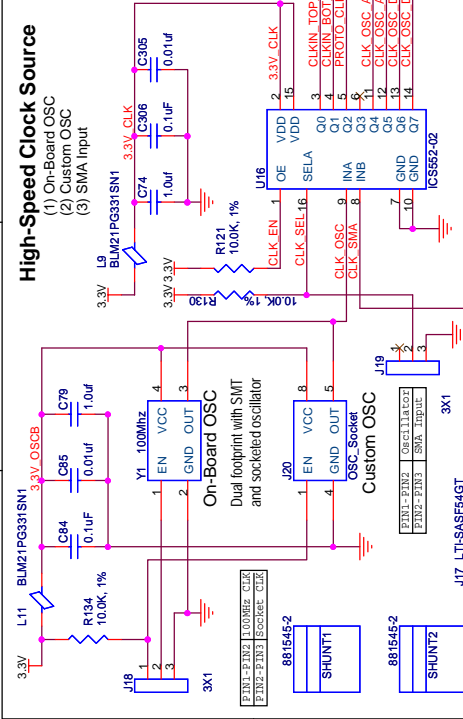
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# Cyclone II Cloning

## High-Speed Clock Source

- (1) On-Board OSC
- (2) Custom OSC
- (3) SMA Input



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# CYCLONE II BANKS 1 & 2

- PROTO\_IO[40..0] 3,19
- PROTO\_CARDBSELn 19
- VGA\_RT[0] 6,15
- VGA\_GT[0] 15
- VGA\_BT[0] 15
- VGA\_CLK 15

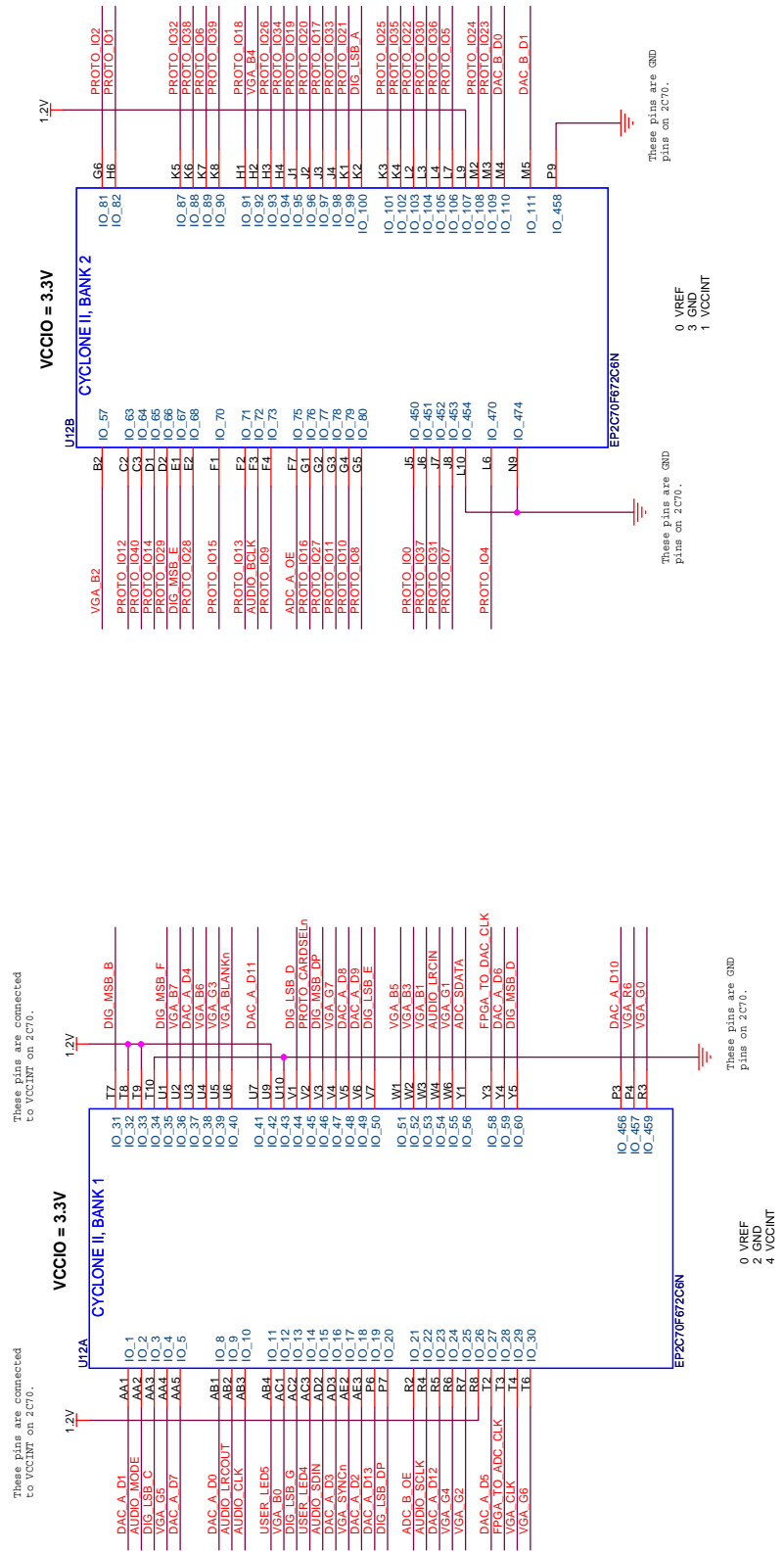
- USER\_LED[7..0] 3,6,10,17
- DIG\_MSB\_B 17
- DIG\_MSB\_E 17
- DIG\_MSB\_F 17
- DIG\_MSB\_G 17
- DIG\_MSB\_DP 17
- DIG\_LSB\_C 17
- DIG\_LSB\_D 17
- DIG\_LSB\_E 17
- DIG\_LSB\_G 17
- DIG\_LSB\_DP 17

- FRGA\_TO\_ADC\_CLK 3
- DAC\_B\_D[13..0] 3,6,14
- ADC\_A\_OE 11

- FRGA\_TO\_DAC\_CLK 3
- DAC\_A\_D[13..0] 13
- ADC\_B\_OE 12

- AUDIO\_BCLK 16
- AUDIO\_SCLK 16
- AUDIO\_CLK 16
- AUDIO\_SDN 16
- AUDIO\_LRCLK 16
- AUDIO\_LRCLK 16
- ADC\_SDATA 11,12

- VGA\_SWCn 15
- VGA\_BLANKn 15



These pins are connected to VCCINT on 2C70.

These pins are GND pins on 2C70.

These pins are connected to VCCINT on 2C70.

These pins are GND pins on 2C70.

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The Cyclone II DSP Board

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Rev C

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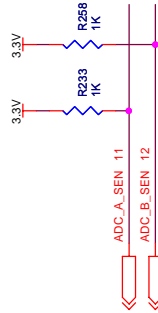


# CYCLONE II BANKS 3 & 4

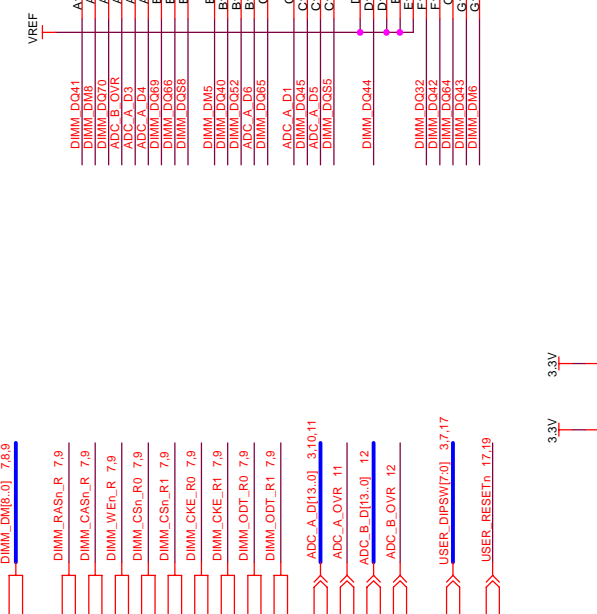
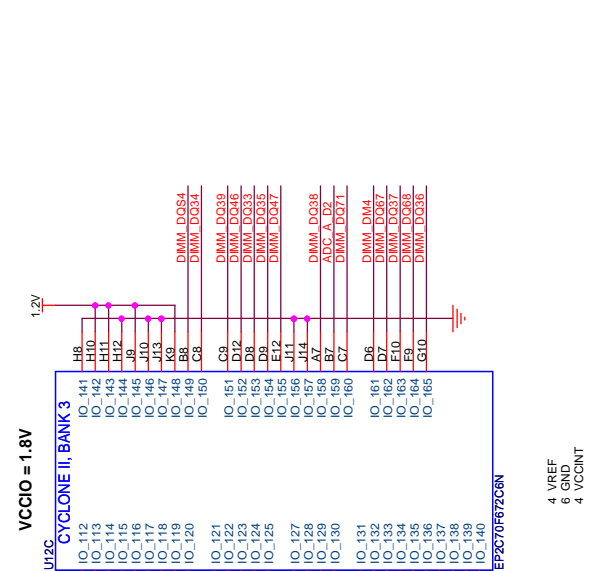
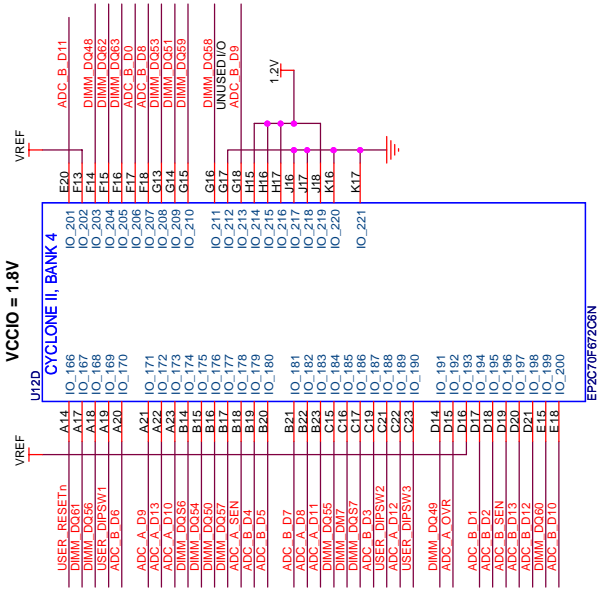
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- ◀◀ DIMM\_DQS[8..0] 7.8.9
- ◀◀ DIMM\_A\_R[15..0] 7.9
- ◀◀ DIMM\_BA\_R[2..0] 7.9
- ◀◀ DIMM\_DM[8..0] 7.8.9

- ◀◀ DIMM\_RASn\_R 7.9
- ◀◀ DIMM\_CASn\_R 7.9
- ◀◀ DIMM\_WEn\_R 7.9
- ◀◀ DIMM\_CSn\_R0 7.9
- ◀◀ DIMM\_CSn\_R1 7.9
- ◀◀ DIMM\_CKE\_R0 7.9
- ◀◀ DIMM\_CKE\_R1 7.9
- ◀◀ DIMM\_ODT\_R0 7.9
- ◀◀ DIMM\_ODT\_R1 7.9

- ◀◀ ADC\_A\_DT[13..0] 3.10.11
- ◀◀ ADC\_A\_OVR 11
- ◀◀ ADC\_B\_DT[13..0] 12
- ◀◀ ADC\_B\_OVR 12
- ◀◀ USER\_DIPSW[7..0] 3.7.17
- ◀◀ USER\_RESETn\_17..19



1.8V driving 3.3V logic must be driven as open-drain



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# CYCLONE II BANKS 5 & 6

DAC.A [13.0] 413  
 DAC.B [13.0] 34,14

EVM\_A[21..2] 18  
 EVM\_D[31..0] 18  
 EVM\_BE[3..0] 18  
 EVM\_INT[3..0] 18  
 EVM\_CE[3..2] 10,18  
 EVM\_DX[0..18]

EVM\_CNTLD 18  
 EVM\_STATO 18  
 EVM\_DMACO 18  
 EVM\_AWEN 18

EVM\_DR0 18  
 EVM\_OEn 18  
 EVM\_ARDY 18  
 EVM\_CLKX0 18  
 EVM\_FSX0 18  
 EVM\_CLKR0 18  
 EVM\_FSR0 18

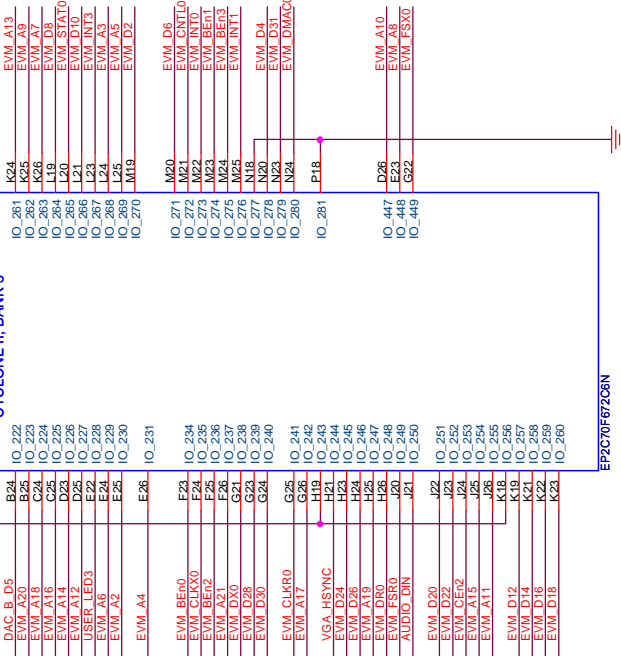
USER\_LED[3..0] 3,4,10,17  
 AUDIO\_CSn 16  
 AUDIO\_DIN 16  
 EVM\_RESET 3,18

VGA\_HSYN 15  
 VGA\_RT[0] 4,15  
 VGA\_BIT[0] 4,15

DIG\_MSB\_A 17  
 DIG\_MSB\_C 17  
 DIG\_MSB\_G 17  
 DIG\_LSB\_B 17  
 DIG\_LSB\_F 17  
 ADC\_RESET 11,12  
 ADC\_SCLK 11,12  
 ADC\_B\_SEN 5,12  
 EPCS\_USER\_CSn 10

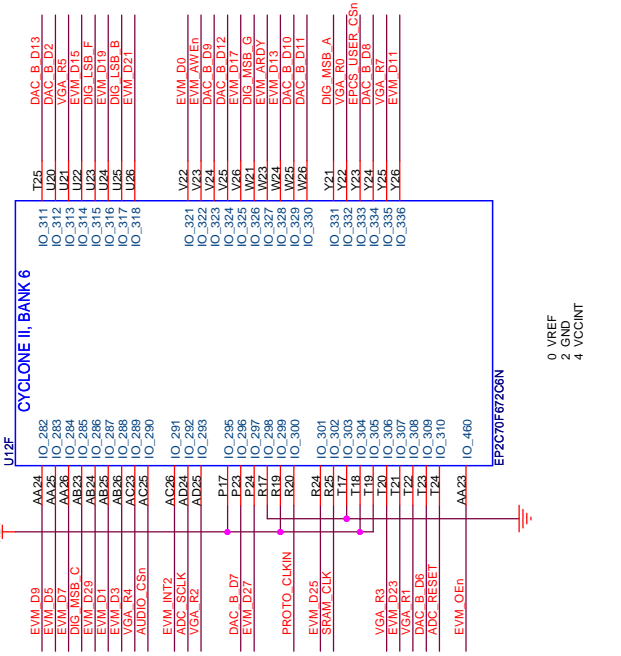
SRAM\_CLK 18  
 PROTO\_CLKIN 19

VCCIO = 3.3V  
 U12F  
 CYCLONE II, BANK 5  
 EP2C70F67Z06N



0 VREF  
 2 GND  
 2 VCCINT

VCCIO = 3.3V  
 U12F  
 CYCLONE II, BANK 6  
 EP2C70F67Z06N



0 VREF  
 2 GND  
 4 VCCINT

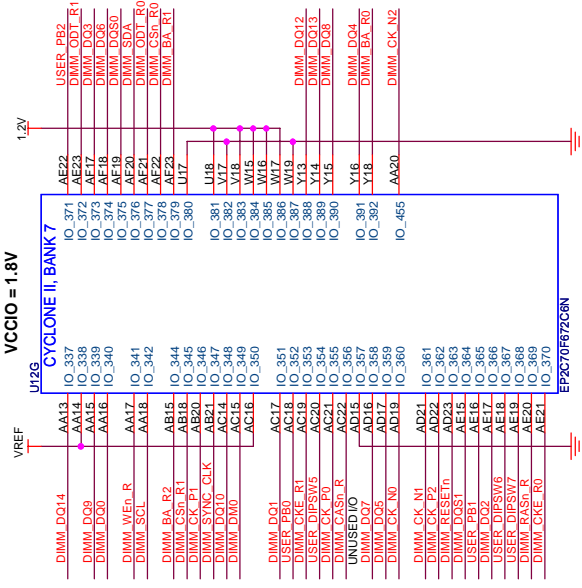
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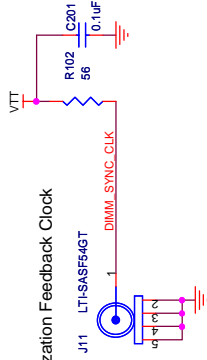
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# CYCLONE II BANKS 7 & 8

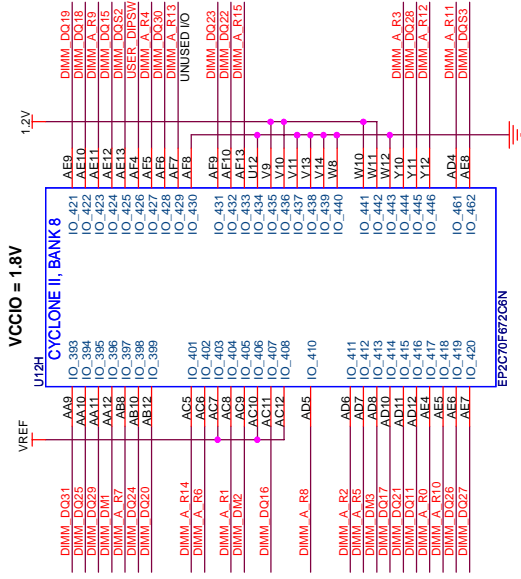
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- << DIMM\_DQS[8..0] 5.8,9
- << DIMM\_A\_R[15..0] 9
- << DIMM\_BA\_R[2..0] 9
- << DIMM\_DM[8..0] 5.8,9
  
- << DIMM\_RASn\_R 9
- << DIMM\_CASn\_R 9
- << DIMM\_WEn\_R 9
- << DIMM\_CSn\_R0 9
- << DIMM\_CSn\_R1 9
- << DIMM\_CKE\_R0 9
- << DIMM\_CKE\_R1 9
- << DIMM\_ODT\_R0 9
- << DIMM\_ODT\_R1 9
- << DIMM\_CK\_P[2..0] 8
- << DIMM\_CK\_N[2..0] 8
- << DIMM\_SDA 8
- << DIMM\_SCL 8
- << DIMM\_RESETn 8
  
- << USER\_PB[3..0] 3,17
- << USER\_DIPS[W7..0] 3,5,17
- << PROTO\_CLKIN 6,19
- << DIMM\_SYNC\_CLK 3



- 2 VREF
- 4 GND
- 5 VCCINT



SMA for External Clock Input / Eye Diagram Output  
(secondary use)



- 3 VREF
- 7 GND
- 4 VCCINT

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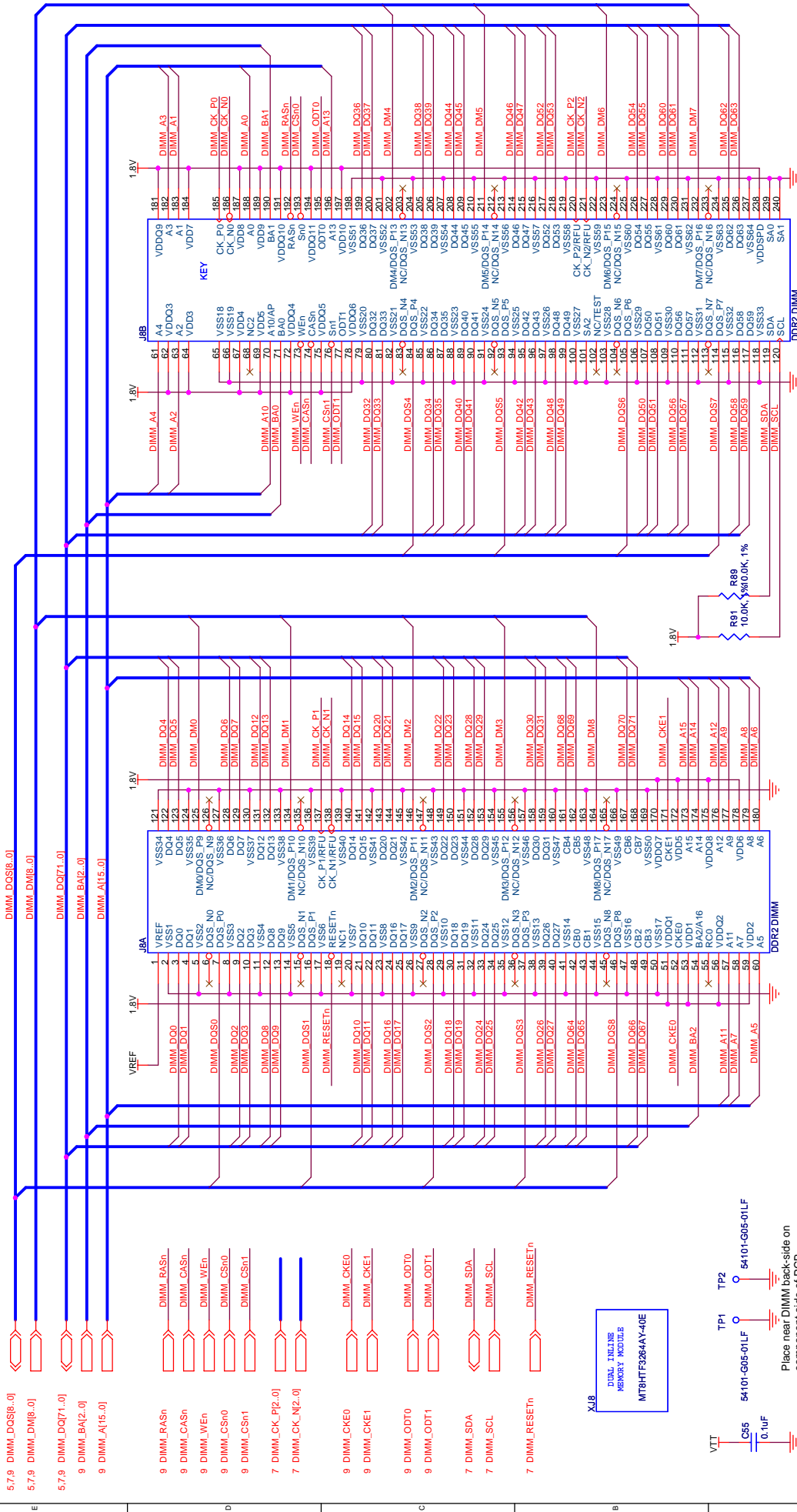
The **Cyclone II DSP Board**

Size B Document Number **150-0310202-C1** Rev C

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# DDR2 SDRAM DIMM



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Place near DIMM back-side on component side of PCB

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- 5.7.8 DIMM\_DQ7(1..0)
- 5.7.8 DIMM\_DQS(8..0)
- 7 DIMM\_A\_R(15..0)
- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
- 7 DIMM\_RASn\_R
- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
- 7 DIMM\_CS0n\_R0
- 7 DIMM\_CS0n\_R1
- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
- 8 DIMM\_CS1
- 8 DIMM\_CKE0
- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

- 5.7.8 DIMM\_DQ7(1..0)
- 5.7.8 DIMM\_DQS(8..0)
- 7 DIMM\_A\_R(15..0)
- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
- 7 DIMM\_RASn\_R
- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
- 7 DIMM\_CS0n\_R0
- 7 DIMM\_CS0n\_R1
- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
- 8 DIMM\_CS1
- 8 DIMM\_CKE0
- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

- 5.7.8 DIMM\_DQ7(1..0)
- 5.7.8 DIMM\_DQS(8..0)
- 7 DIMM\_A\_R(15..0)
- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
- 7 DIMM\_RASn\_R
- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
- 7 DIMM\_CS0n\_R0
- 7 DIMM\_CS0n\_R1
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- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
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- 8 DIMM\_CASn
- 8 DIMM\_WEn
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- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

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- 5.7.8 DIMM\_DQS(8..0)
- 7 DIMM\_A\_R(15..0)
- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
- 7 DIMM\_RASn\_R
- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
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- 7 DIMM\_CS0n\_R1
- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
- 8 DIMM\_CS1
- 8 DIMM\_CKE0
- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

- 5.7.8 DIMM\_DQ7(1..0)
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- 7 DIMM\_RASn\_R
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- 7 DIMM\_RASn\_R
- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
- 7 DIMM\_CS0n\_R0
- 7 DIMM\_CS0n\_R1
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- 7 DIMM\_CKE\_R1
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- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
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- 8 DIMM\_CKE0
- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

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- 5.7.8 DIMM\_DQS(8..0)
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- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
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- 7 DIMM\_CASn\_R
- 7 DIMM\_WEn\_R
- 7 DIMM\_CS0n\_R0
- 7 DIMM\_CS0n\_R1
- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
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- 8 DIMM\_ODT0
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- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
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- 7 DIMM\_CS0n\_R0
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- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
- 8 DIMM\_CS1
- 8 DIMM\_CKE0
- 8 DIMM\_CKE1
- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

- 5.7.8 DIMM\_DQ7(1..0)
- 5.7.8 DIMM\_DQS(8..0)
- 7 DIMM\_A\_R(15..0)
- 7 DIMM\_BA\_R(2..0)
- 5.7.8 DIMM\_DM(8..0)
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- 7 DIMM\_CS0n\_R1
- 7 DIMM\_CKE\_R0
- 7 DIMM\_CKE\_R1
- 7 DIMM\_ODT\_R0
- 7 DIMM\_ODT\_R1
- 8 DIMM\_AH(15..0)
- 8 DIMM\_BA(2..0)
- 8 DIMM\_RASn
- 8 DIMM\_CASn
- 8 DIMM\_WEn
- 8 DIMM\_CS0
- 8 DIMM\_CS1
- 8 DIMM\_CKE0
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- 8 DIMM\_ODT0
- 8 DIMM\_ODT1

### DDR2 SDRAM DIMM Terminations

### II-Side Termination Resistors

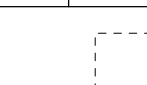
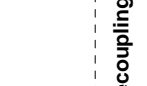
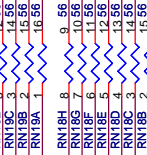
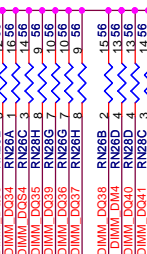
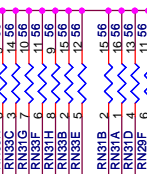
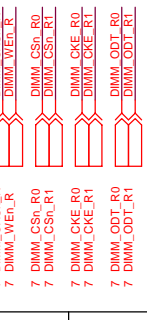
### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors



### III-Side Termination Resistors

### II-Side Termination Resistors

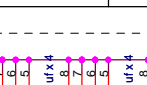
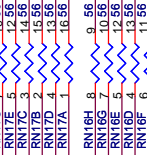
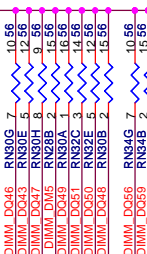
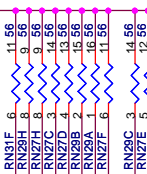
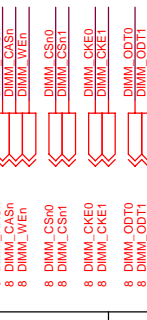
### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors



### III-Side Termination Resistors

### II-Side Termination Resistors

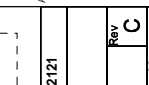
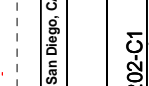
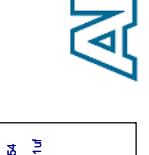
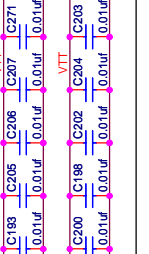
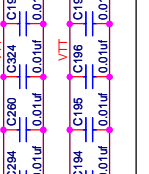
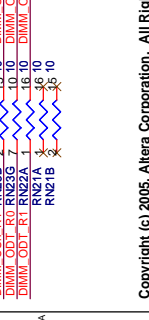
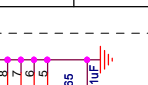
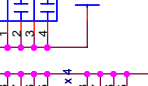
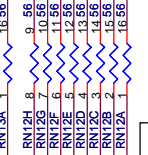
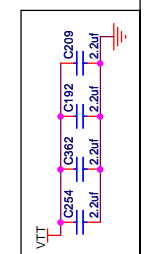
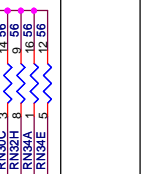
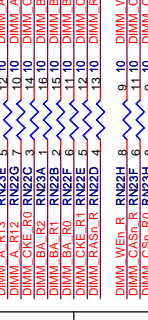
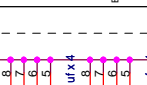
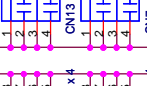
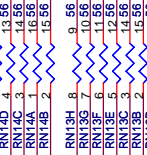
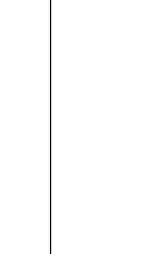
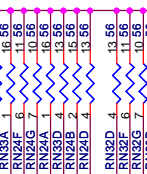
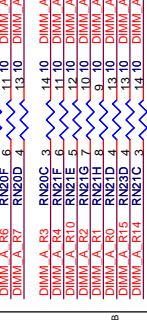
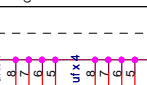
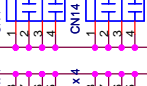
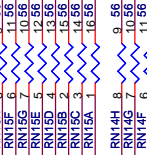
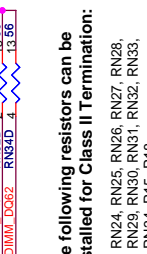
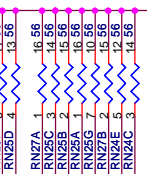
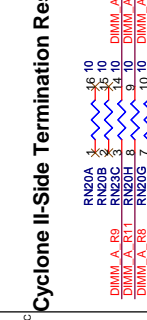
### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors

### II-Side Termination Resistors

### III-Side Termination Resistors



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The Cyclone II DSP Board

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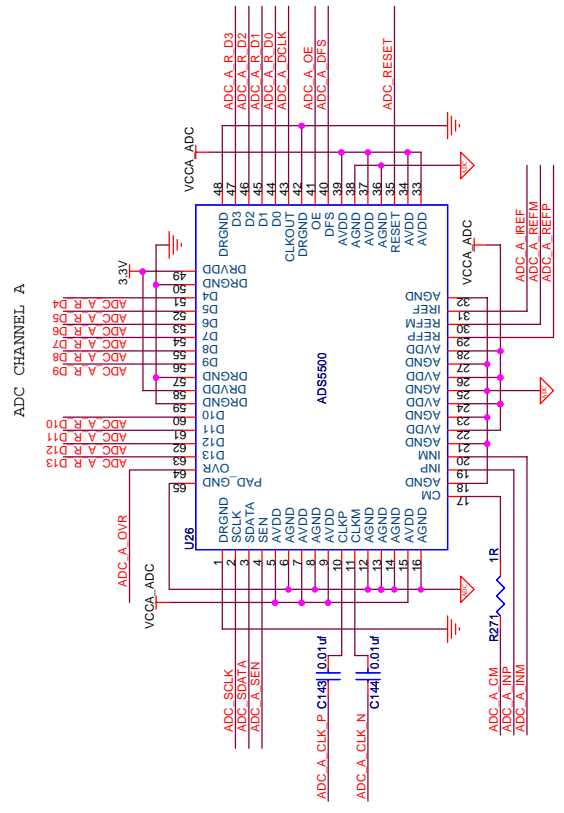
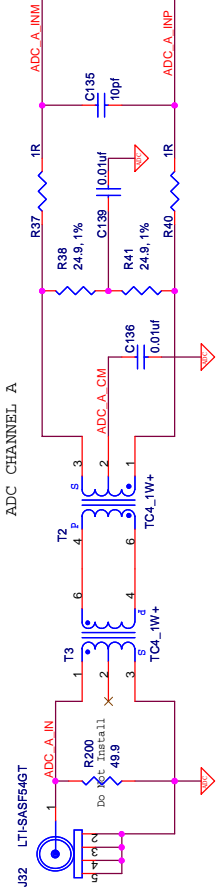
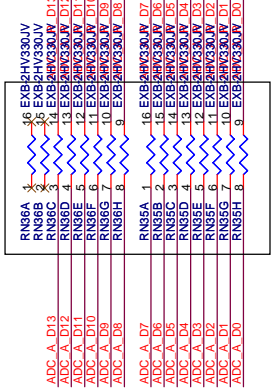
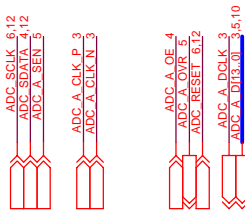
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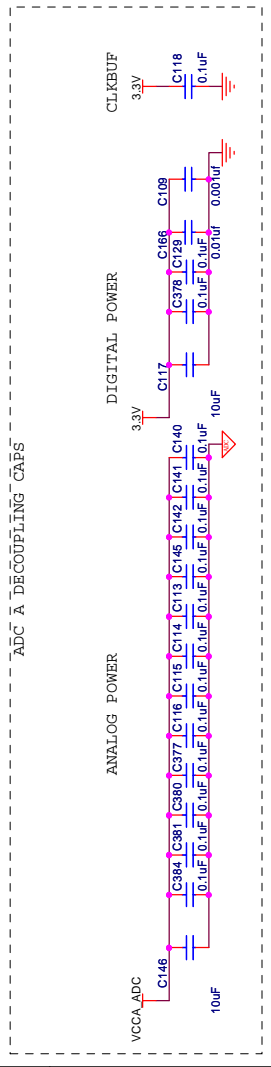
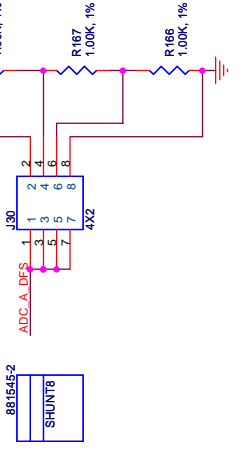




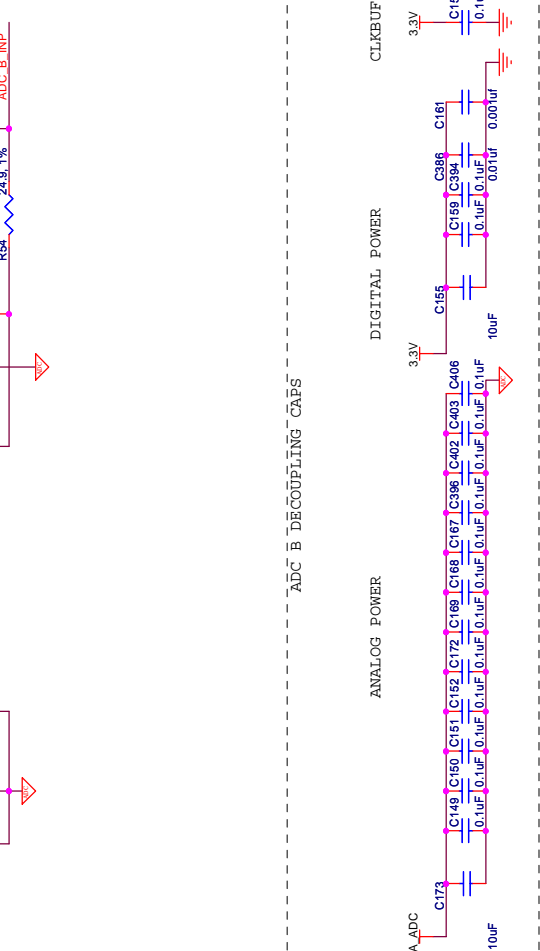
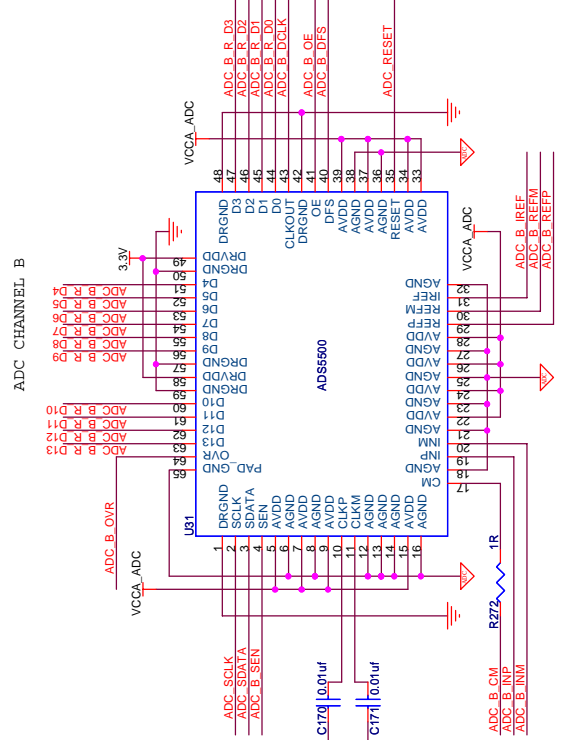
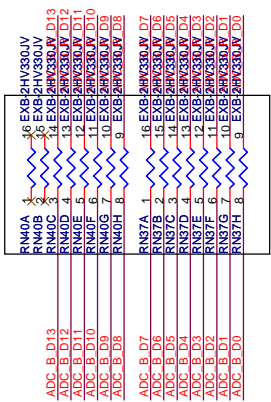
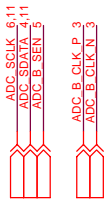
# ADC Channel A



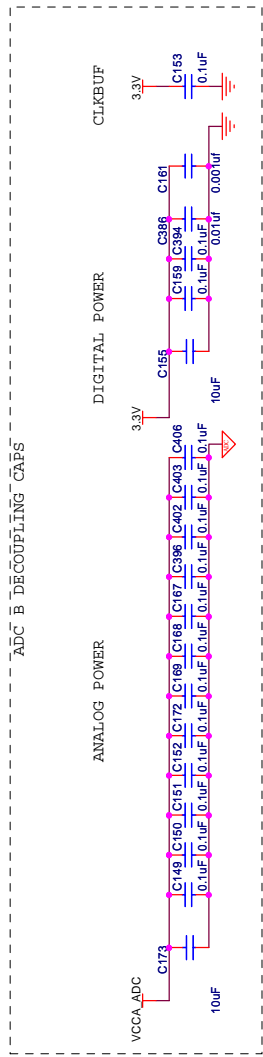
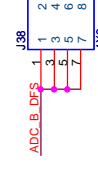
J30 Position	Data Output Format
Pin 1-2	2's Complement data valid falling edge
Pin 3-4	Straight Binary data valid falling edge
Pin 5-6	2's Complement data valid rising edge
Pin 7-8	Straight Binary data valid rising edge



# ADC Channel B



J38 Position	Data Output Format
Pin 1-2	2's Complement data valid falling edge
Pin 3-4	Straight Binary data valid falling edge
Pin 5-6	2's Complement data valid rising edge
Pin 7-8	Straight Binary data valid rising edge



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The Cyclone II DSP Board

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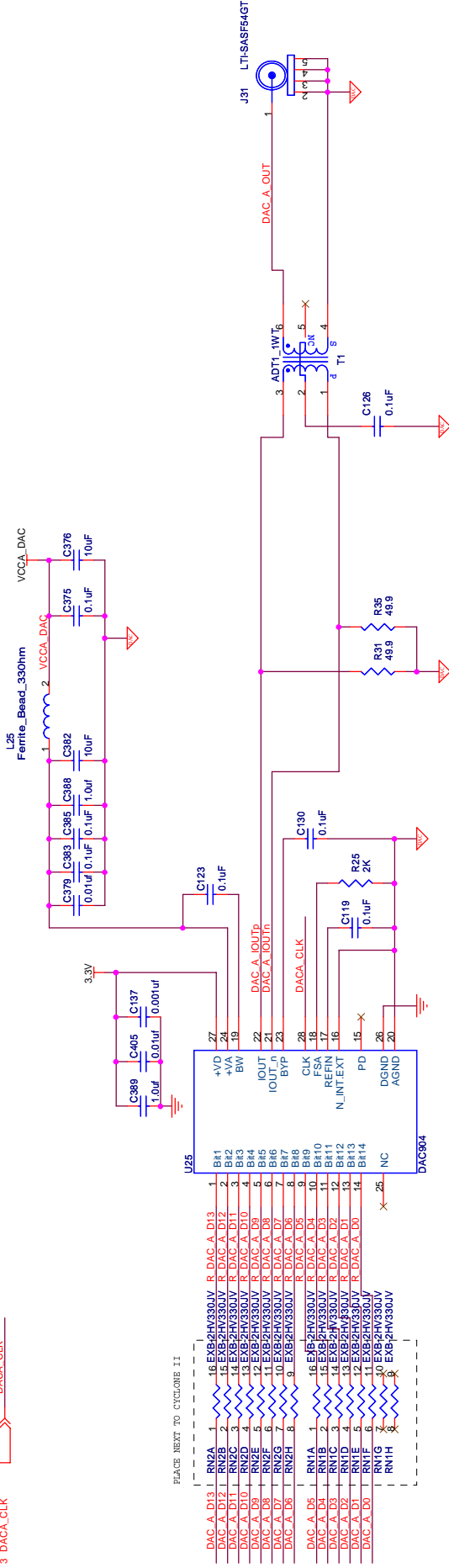
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# DAC CHANNEL A

4 DAC\_A\_D[13:0]

3 DAC\_A\_CLK



PLACES NEXT TO CYCLONE II

DAC A D13	1	RMZA	1	16	EXB2HV330UV	R	DAC A D13
DAC A D12	2	RNZA	2	15	EXB2HV330UV	R	DAC A D12
DAC A D11	3	RNZB	3	14	EXB2HV330UV	R	DAC A D11
DAC A D10	4	RNZD	4	13	EXB2HV330UV	R	DAC A D10
DAC A D9	5	RNZF	5	12	EXB2HV330UV	R	DAC A D9
DAC A D8	6	RNZG	6	11	EXB2HV330UV	R	DAC A D8
DAC A D7	7	RNZH	7	10	EXB2HV330UV	R	DAC A D7
DAC A D6	8	RNZH	8	9	EXB2HV330UV	R	DAC A D6
DAC A D5	9	RN1A	1	16	EXB2HV330UV	R	DAC A D4
DAC A D4	10	RN1B	2	15	EXB2HV330UV	R	DAC A D3
DAC A D3	11	RN1C	3	14	EXB2HV330UV	R	DAC A D2
DAC A D2	12	RN1D	4	13	EXB2HV330UV	R	DAC A D1
DAC A D1	13	RN1E	5	12	EXB2HV330UV	R	DAC A D0
DAC A D0	14	RN1F	6	11	EXB2HV330UV	R	DAC A D0
DAC A D0	14	RN1G	7	10	EXB2HV330UV	R	DAC A D0
DAC A D0	14	RN1H	8	9	EXB2HV330UV	R	DAC A D0

DAC\_A\_IOUTn TP4  
54101-016-01LF

<Variant Name>

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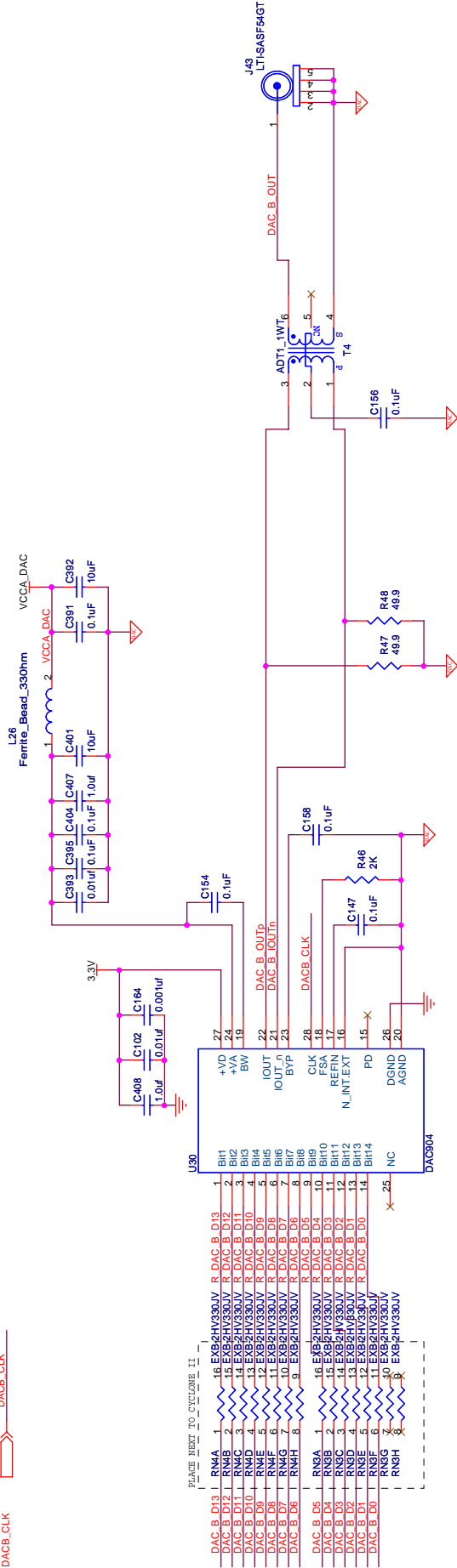



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# DAC CHANNEL B

3,4,6 DAC\_B\_D[13:0] 

3 DACB\_CLK 



DAC\_B\_IOUTn  TP3  
54101-005-01LF

PLACE NEXT TO CYCLOPS II -

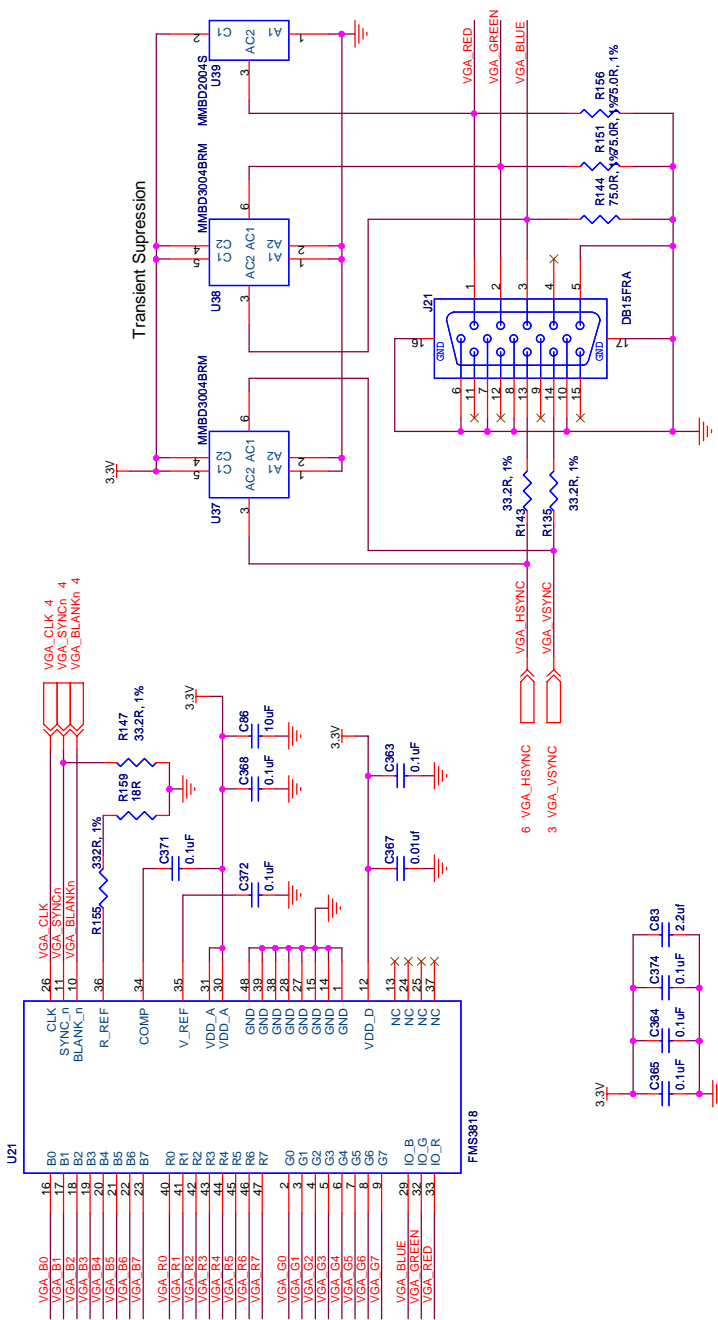
DAC_B_D13	RMA	1	EXB2HV330JV	R	DAC_B_D13
DAC_B_D12	RMAB	2	EXB2HV330JV	R	DAC_B_D12
DAC_B_D11	RMAC	3	EXB2HV330JV	R	DAC_B_D11
DAC_B_D10	RMAD	4	EXB2HV330JV	R	DAC_B_D10
DAC_B_D9	RM4E	5	EXB2HV330JV	R	DAC_B_D9
DAC_B_D8	RM4F	6	EXB2HV330JV	R	DAC_B_D8
DAC_B_D7	RM4G	7	EXB2HV330JV	R	DAC_B_D7
DAC_B_D6	RM4H	8	EXB2HV330JV	R	DAC_B_D6
DAC_B_D5	RM4A	1	EXB2HV330JV	R	DAC_B_D5
DAC_B_D4	RM4B	2	EXB2HV330JV	R	DAC_B_D4
DAC_B_D3	RM4C	3	EXB2HV330JV	R	DAC_B_D3
DAC_B_D2	RM4D	4	EXB2HV330JV	R	DAC_B_D2
DAC_B_D1	RM4E	5	EXB2HV330JV	R	DAC_B_D1
DAC_B_D0	RM4F	6	EXB2HV330JV	R	DAC_B_D0
	RM4G	7	EXB2HV330JV	R	DAC_B_D0
	RM4H	8	EXB2HV330JV	R	DAC_B_D0
	RM4A	1	EXB2HV330JV	R	DAC_B_D0
	RM4B	2	EXB2HV330JV	R	DAC_B_D0
	RM4C	3	EXB2HV330JV	R	DAC_B_D0
	RM4D	4	EXB2HV330JV	R	DAC_B_D0
	RM4E	5	EXB2HV330JV	R	DAC_B_D0
	RM4F	6	EXB2HV330JV	R	DAC_B_D0
	RM4G	7	EXB2HV330JV	R	DAC_B_D0
	RM4H	8	EXB2HV330JV	R	DAC_B_D0
	RM4A	1	EXB2HV330JV	R	DAC_B_D0
	RM4B	2	EXB2HV330JV	R	DAC_B_D0
	RM4C	3	EXB2HV330JV	R	DAC_B_D0
	RM4D	4	EXB2HV330JV	R	DAC_B_D0
	RM4E	5	EXB2HV330JV	R	DAC_B_D0
	RM4F	6	EXB2HV330JV	R	DAC_B_D0
	RM4G	7	EXB2HV330JV	R	DAC_B_D0
	RM4H	8	EXB2HV330JV	R	DAC_B_D0



<Variant Name>  
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# VIDEO DAC

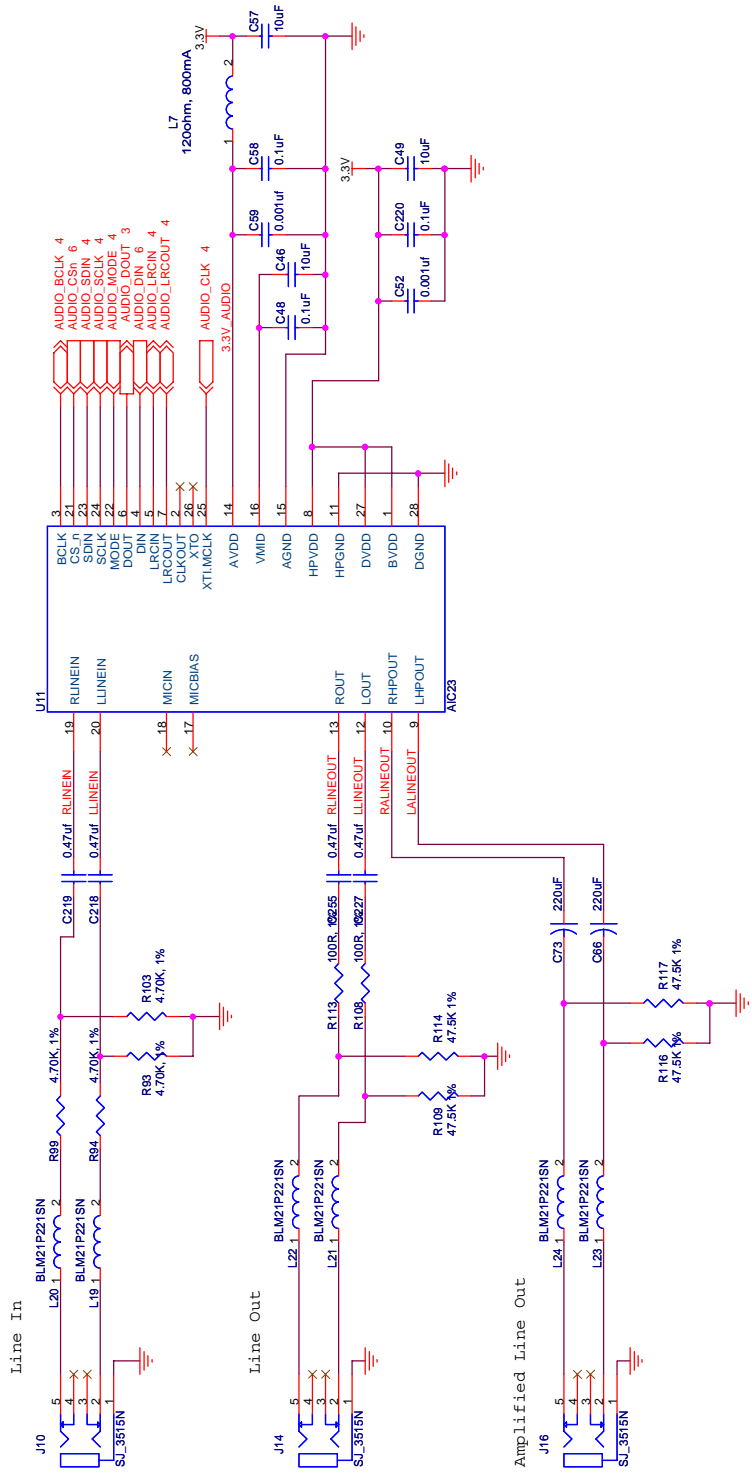
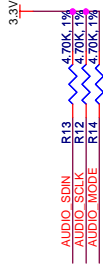
- 4 VGA\_B[7..0]
- 4.6 VGA\_R[7..0]
- 4 VGA\_G[7..0]



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# AIC23 AUDIO CODEC



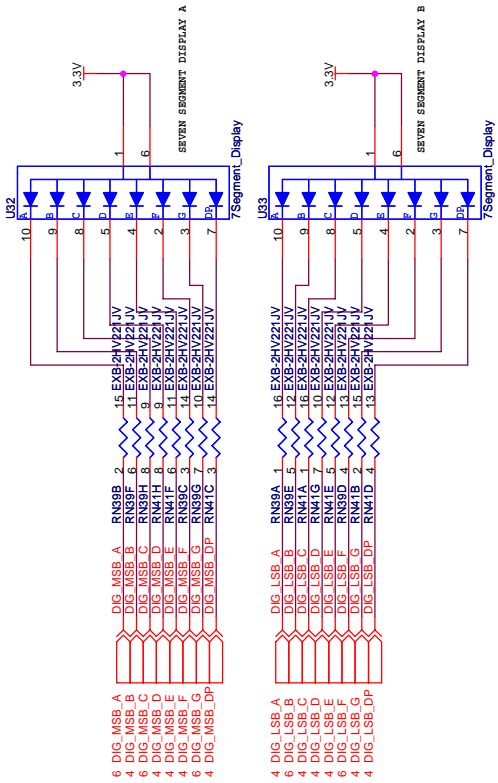
Altera Corporation, 9530 Scranton Rd #400, San Diego, CA 92121	
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# USER IO

## 7-Segment Displays



USER\_PB3\_0] USER\_PB3\_0] 3,7

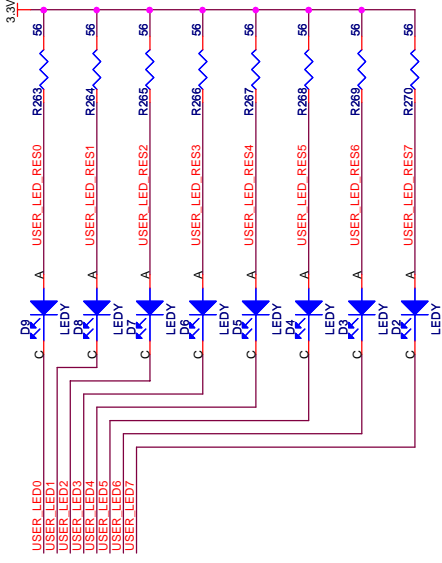
SYS\_RESETn SYS\_RESETn 10

USER\_RESETn USER\_RESETn 5,19

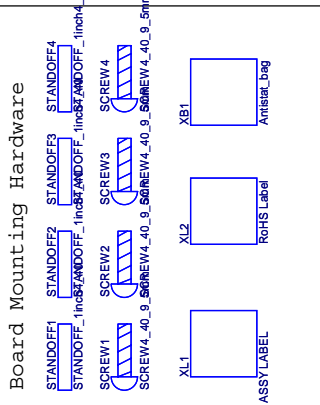
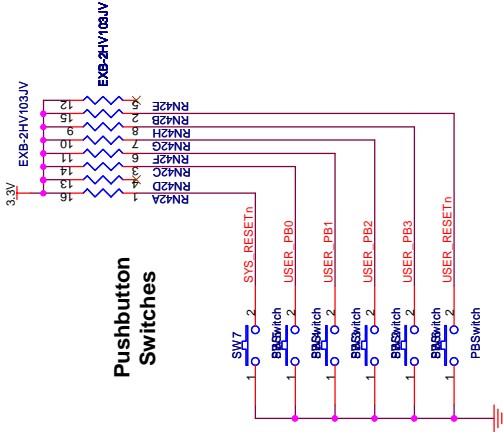
USER\_LED7\_0] USER\_LED7\_0] 3,4,6,10

3.5,7 USER\_DIPSWT0] USER\_DIPSWT0]

## User LEDs



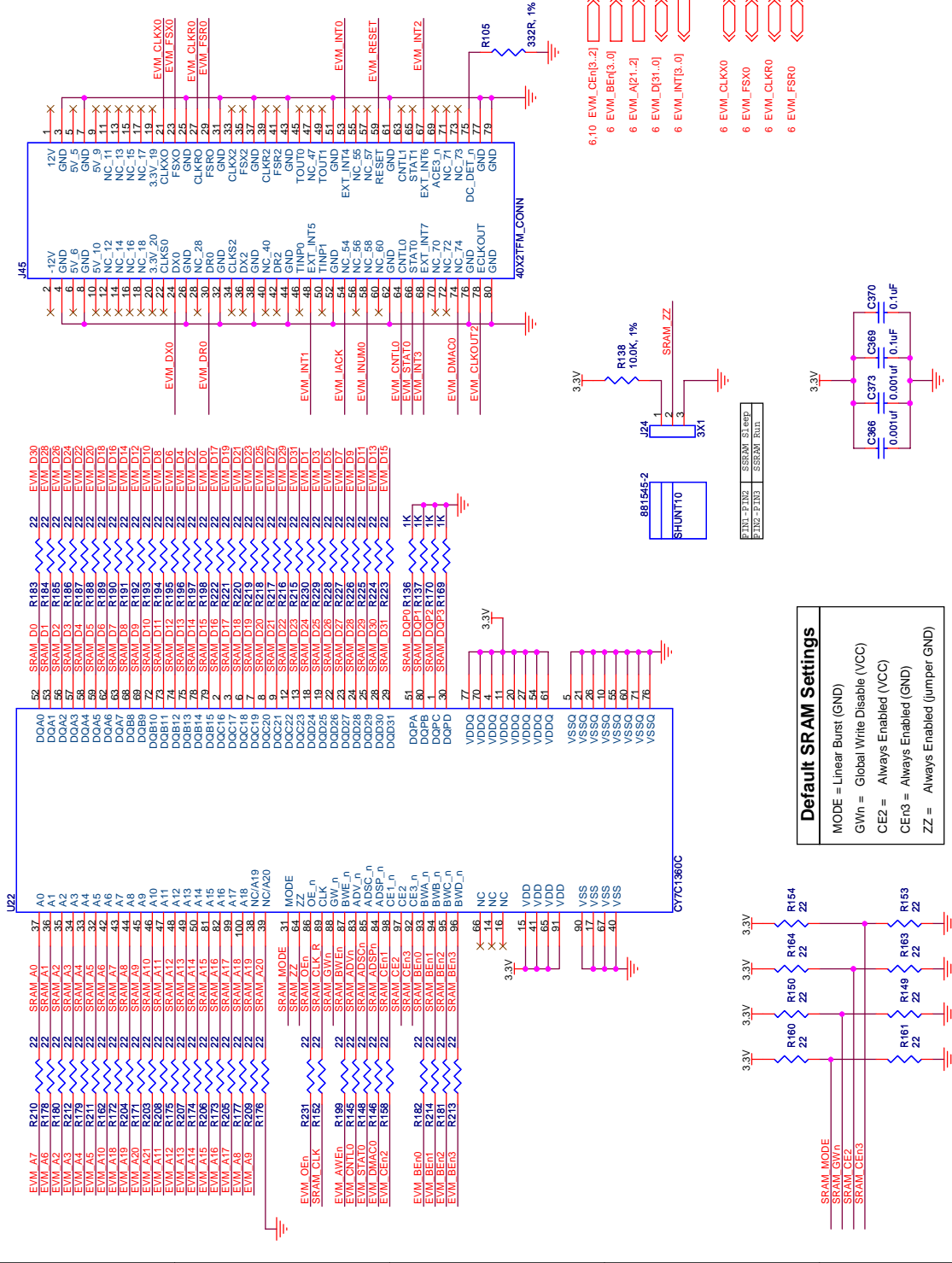
## Pushbutton Switches



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# SSRAM, TI EVM Connectors



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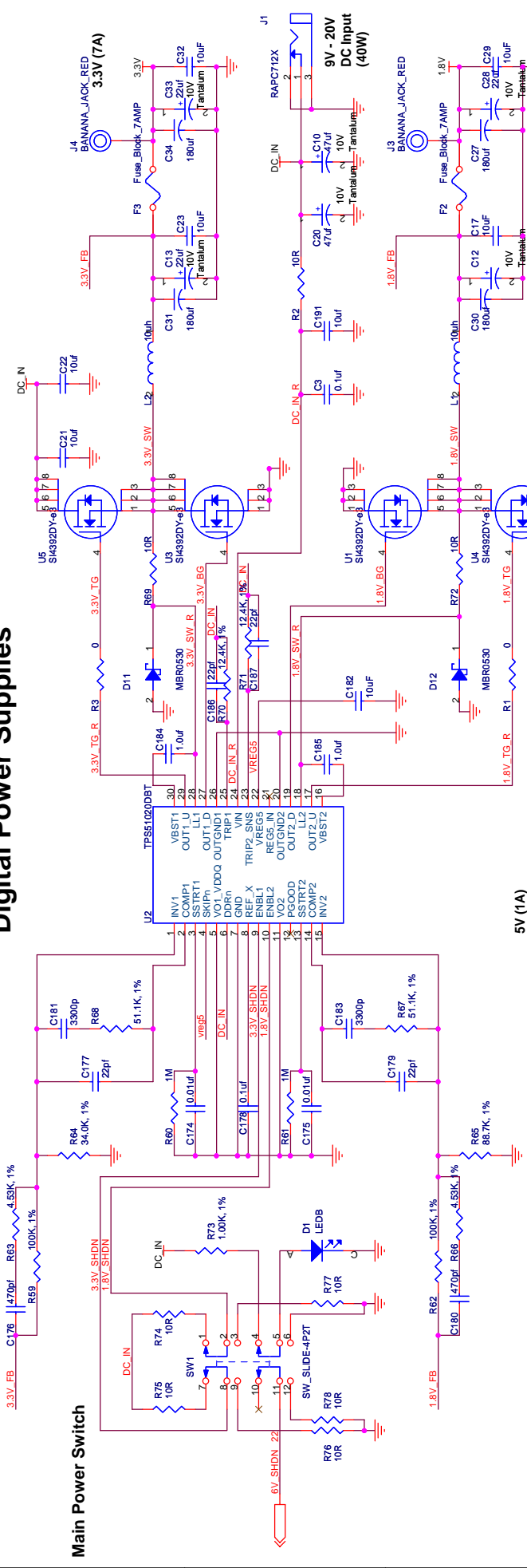




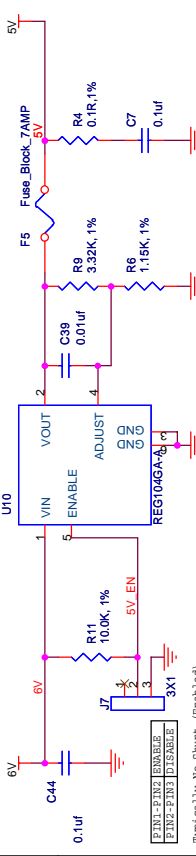


# Digital Power Supplies

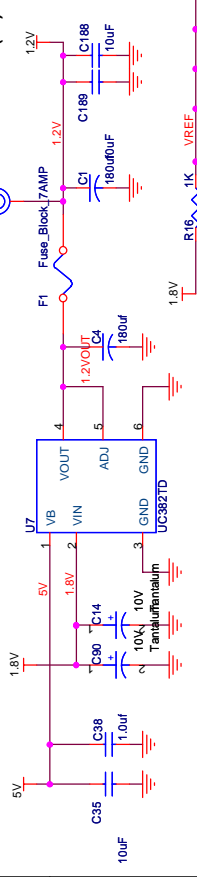
## Main Power Switch



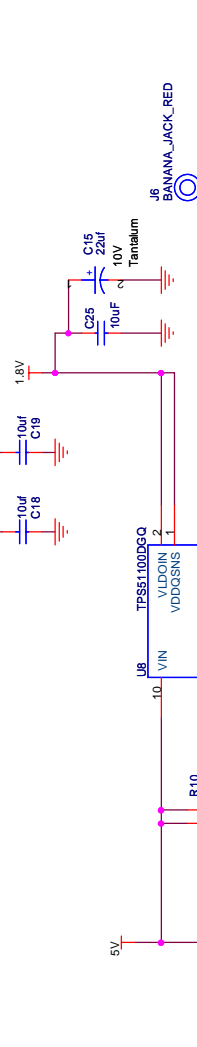
## 5V (1A)



## 1.2V (3A)



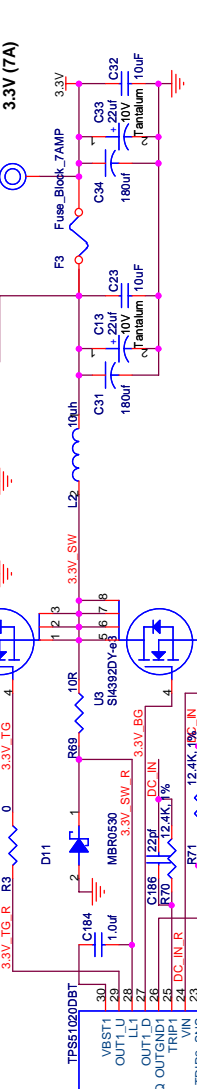
## 1.8V (7A)



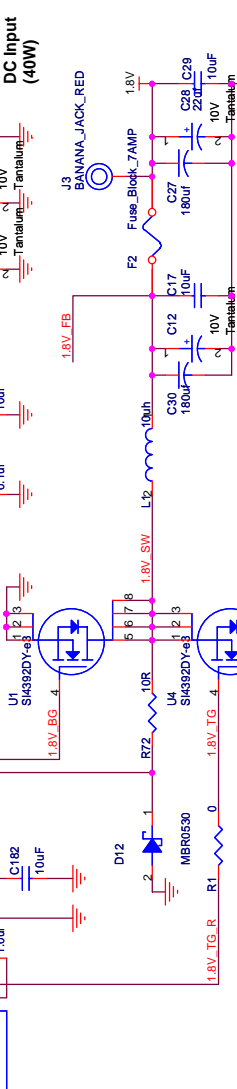
## 0.9V (3A Sink/Src)



## 3.3V (7A)

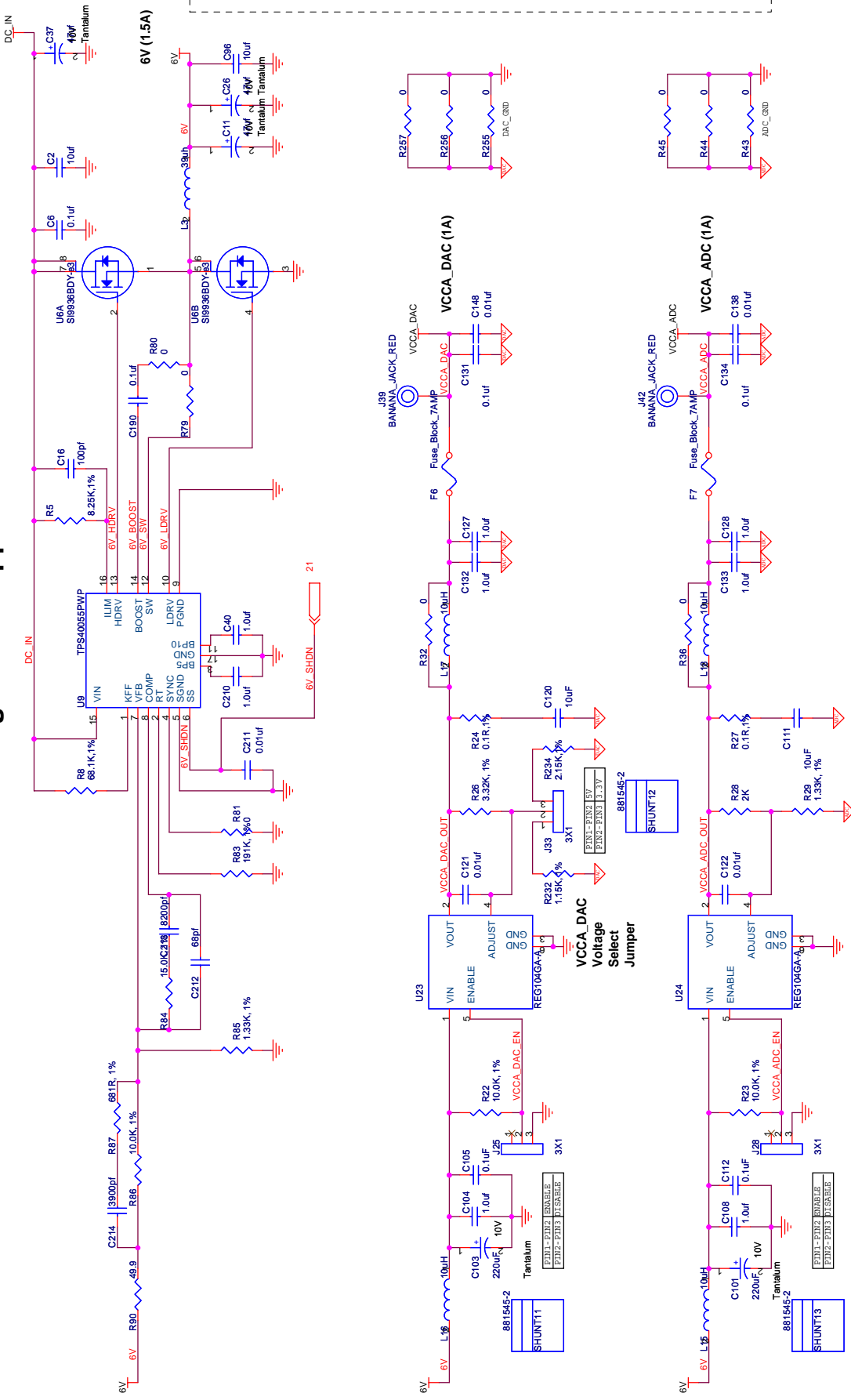


## 9V - 20V DC Input (40W)



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# Analog Power Supplies



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