Layout Verification

of an Inverter Circuit

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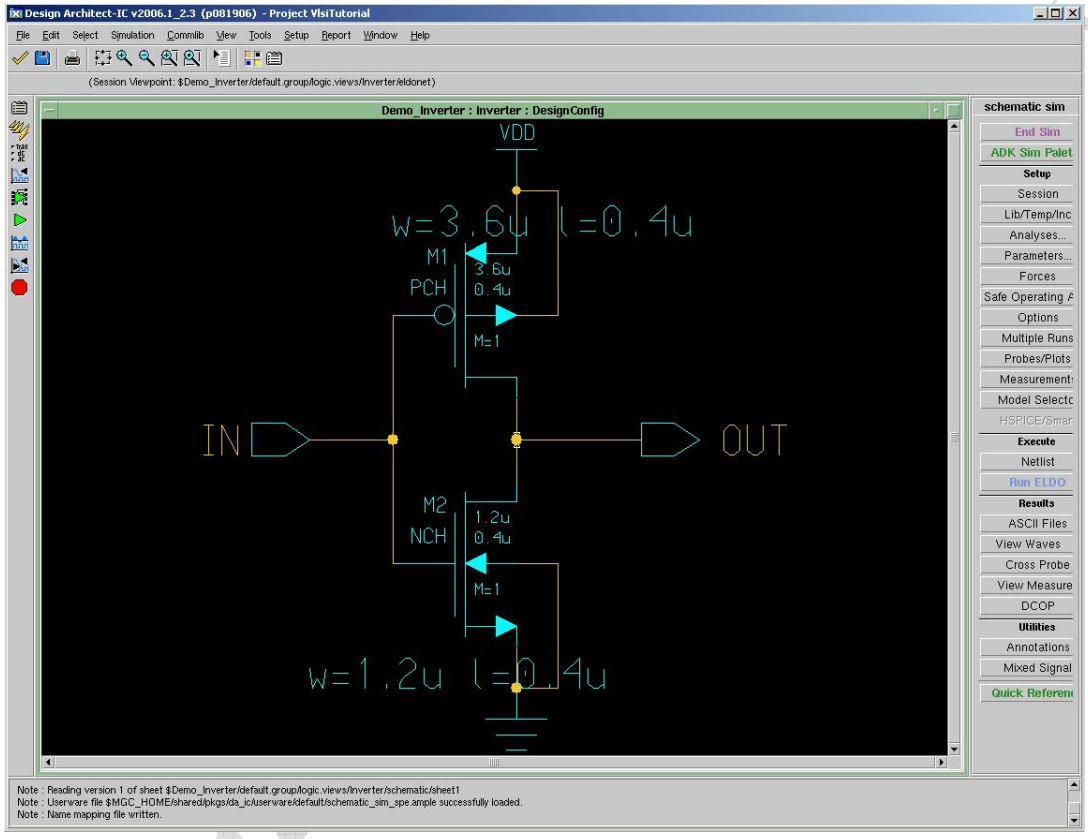
1. Objective

This tutorial shows a step-by-step procedure for verification of a simple digital inverter cell including Design Rule Check (DRC), Layout vs Schematic (LVS).

The following schematic was drawn in a previous tutorial:



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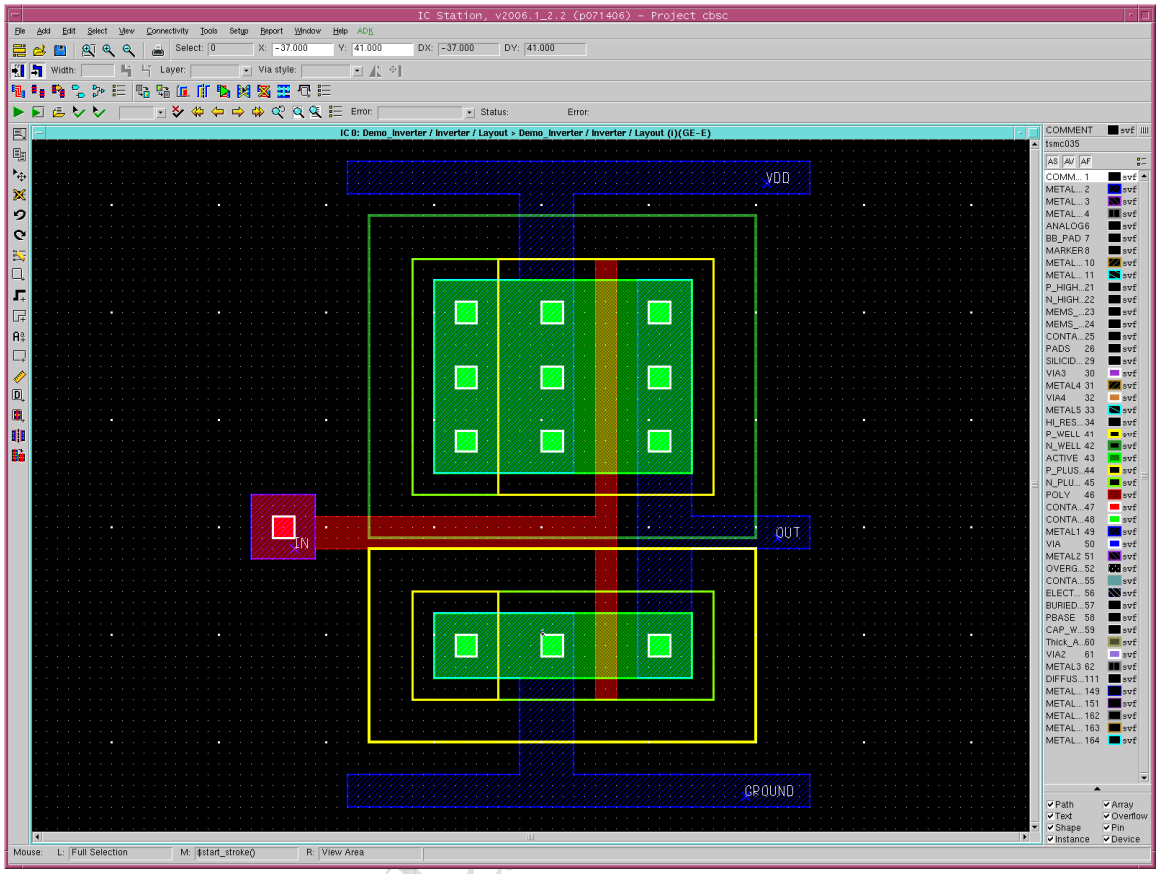
The layout associated with this circuit was drawn in the second tutorial:



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2. Setup & Preparation

The set of directives listed below is applicable to users of the ***Engineering Design Center at Santa Clara University.*** If you are working in a different environment please check with your system administrator.

The steps below are necessary only for the first time to setup the Mentor Graphics environment by changing the settings in your .profile file.
Add the following lines in your **.profile**:

setup mentor-2008.1
alias swd="export MGC_WD=\'pwd\'"

Remember to execute

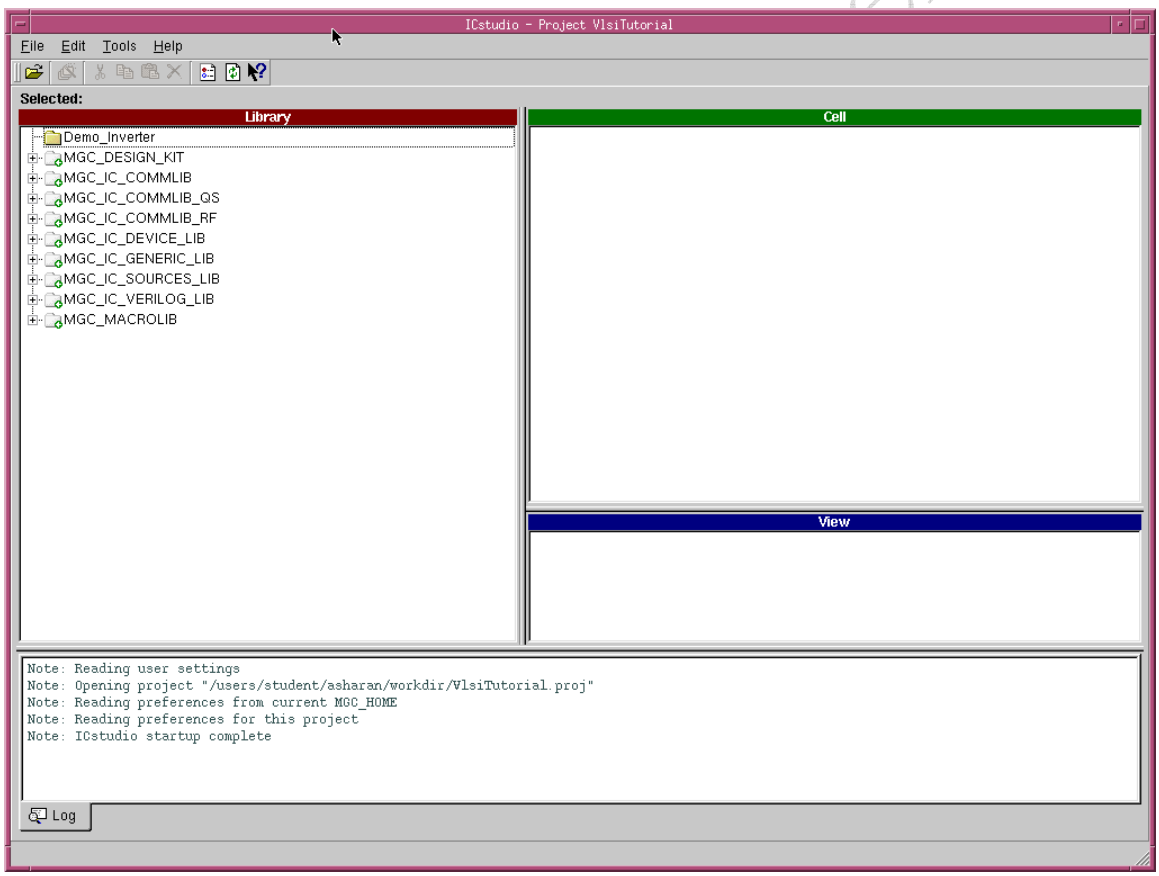
$. profile

3. Launching IC Studio

On the command line

- To Create a directory to contain your projects type: **"mkdir Tutorial"**
- To change the current directory to Tutorial type: **"cd Tutorial".**
- To open ICSTUDIO type: **"icstudio".**

This launches the ICStudio window shown below.



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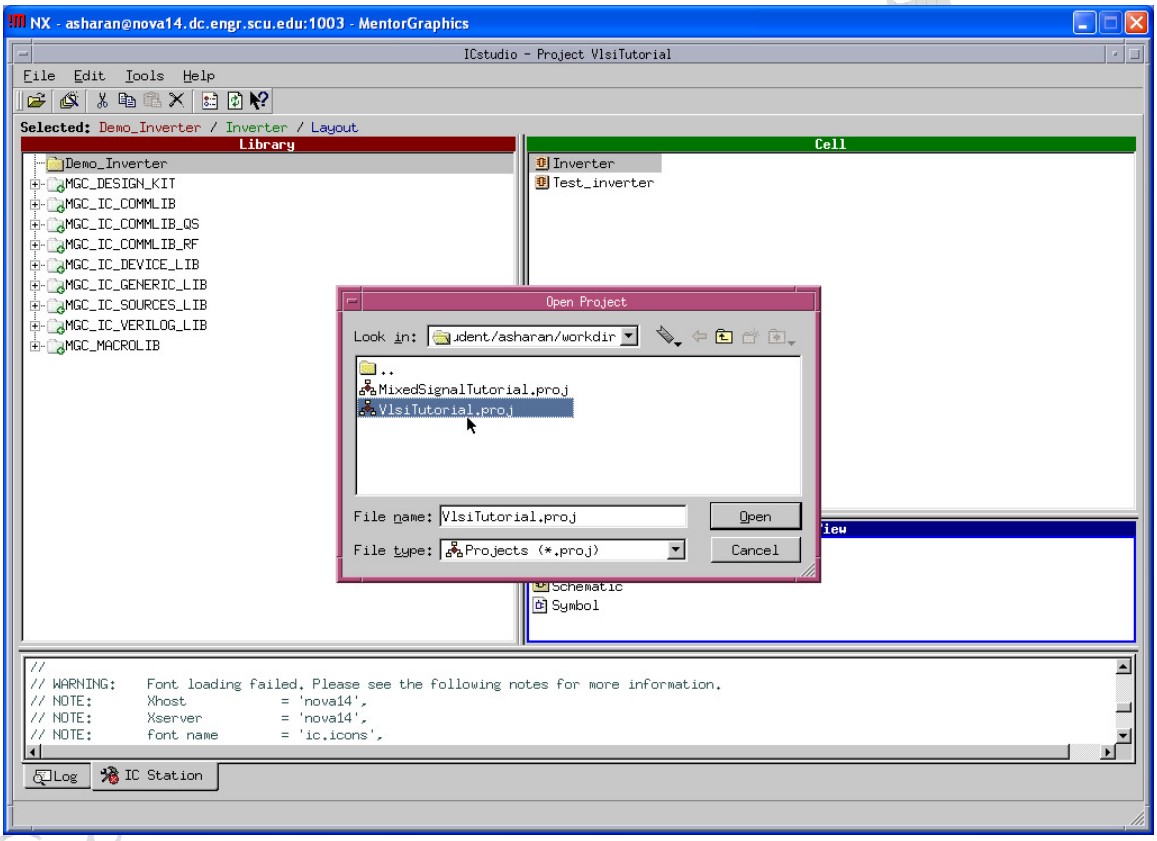
4. Opening the Project

To create a project the follow the three steps given below:

1. Opening icstudio and opening the project

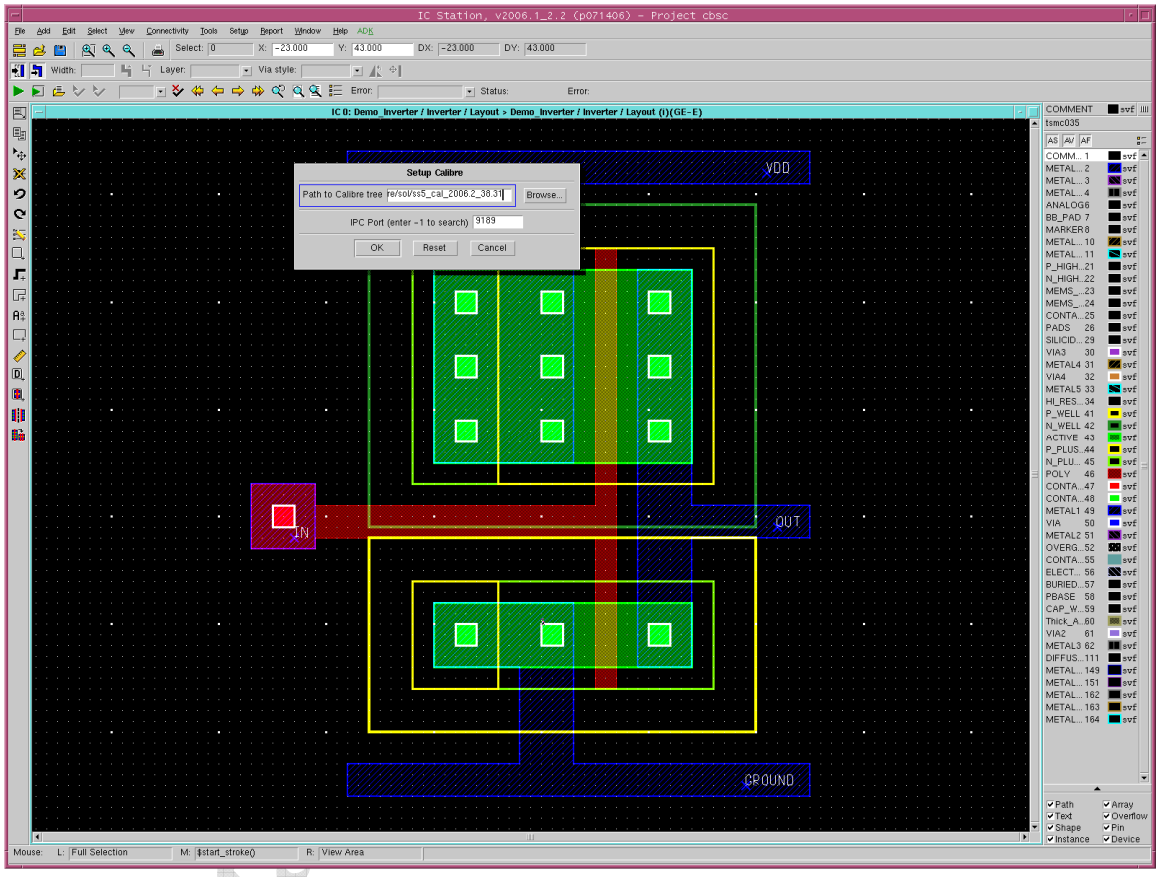
On the ICStudio Window

- Click **File -> Open -> Project** to create a new project.
- Enter the **Project name** (e.g vlsi_tutorial) and the **Project Location**
- Click **Open** in the **Open Project** pop-up window
- When the project opens, double-click on the **Layout** view to launch ICStudio and view your circuit layout.



5. Verifying the Layout Design rules (DRC)

From the menu, select **Calibre > Run DRC**
In the window that pops up, enter the **Path to Calibre as:**
/opt/mentor-2008.1/adk3_1/technology/ic/process/tsmc035.rules



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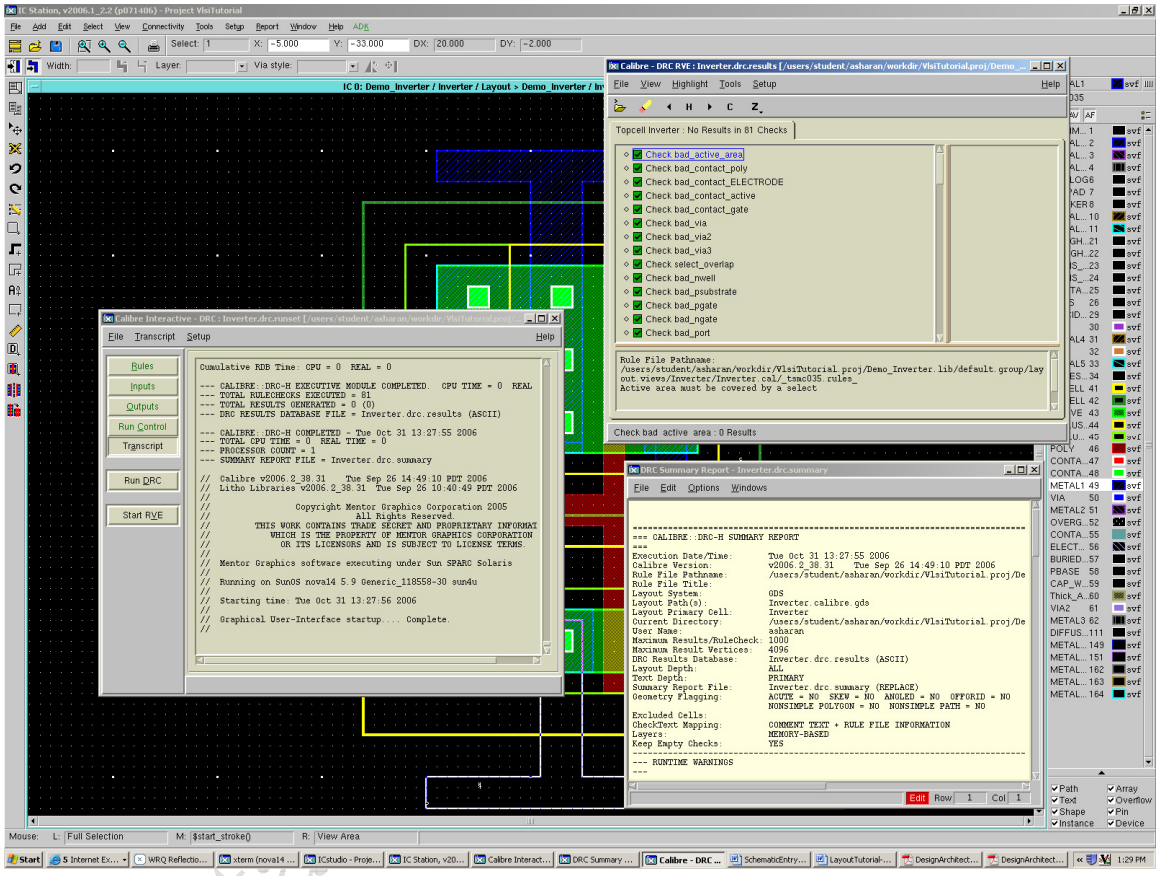
The DRC tool stores results as shown under. Click on **Outputs** to see the location where the tool stores the result

Click **Run DRC**



The **Calibre DRC RVE** should say **No (Zero) Results in 81 Checks** as under
If you do not have any DRC errors the window would look like:

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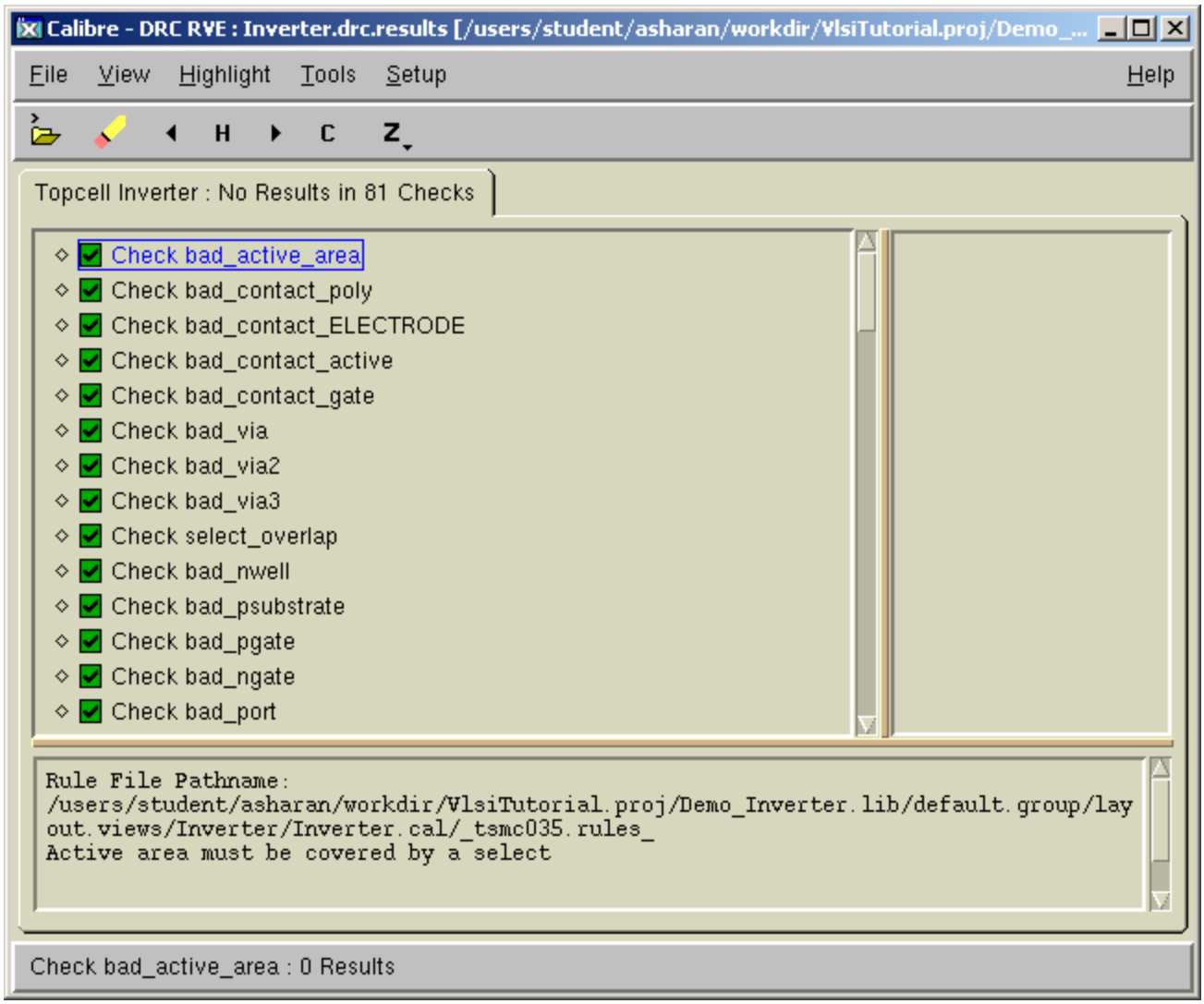
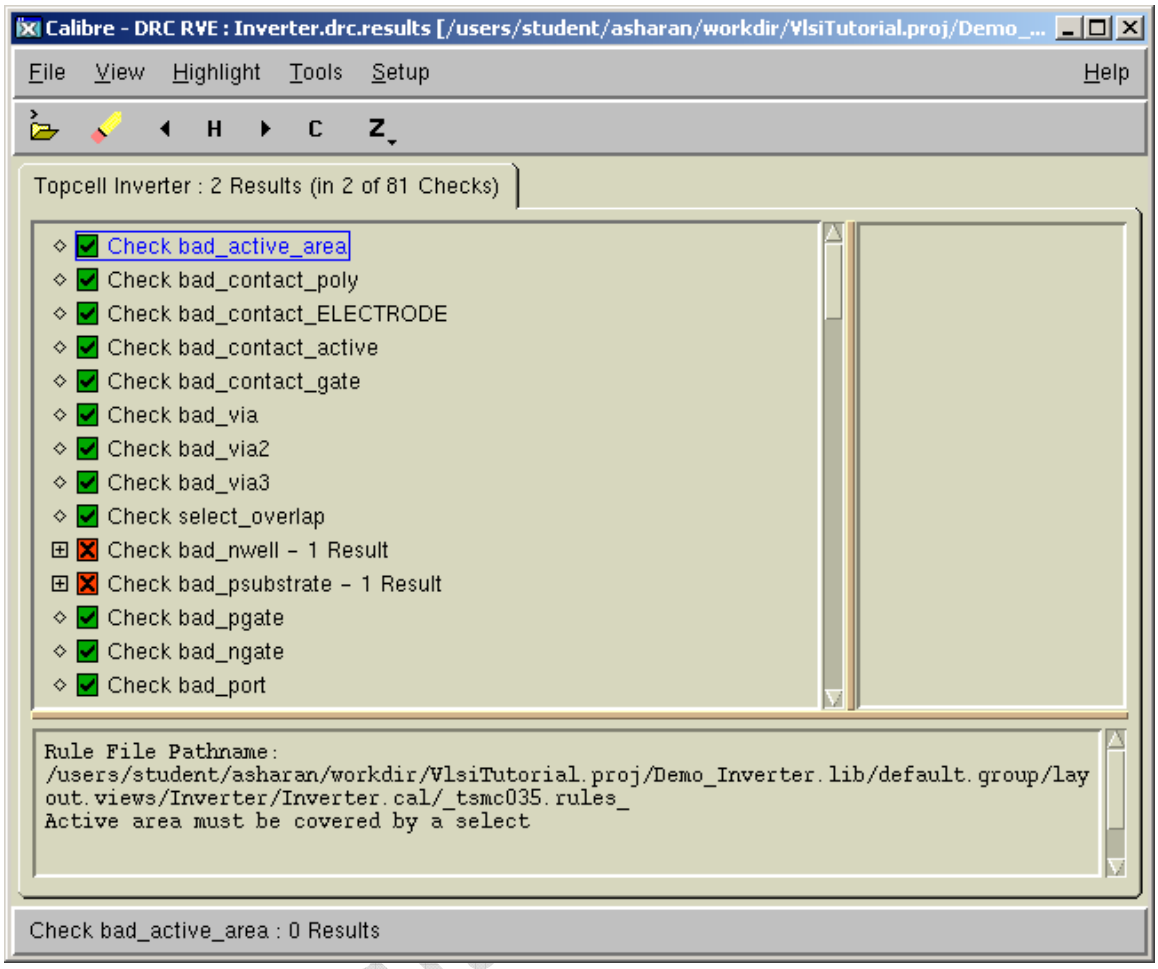
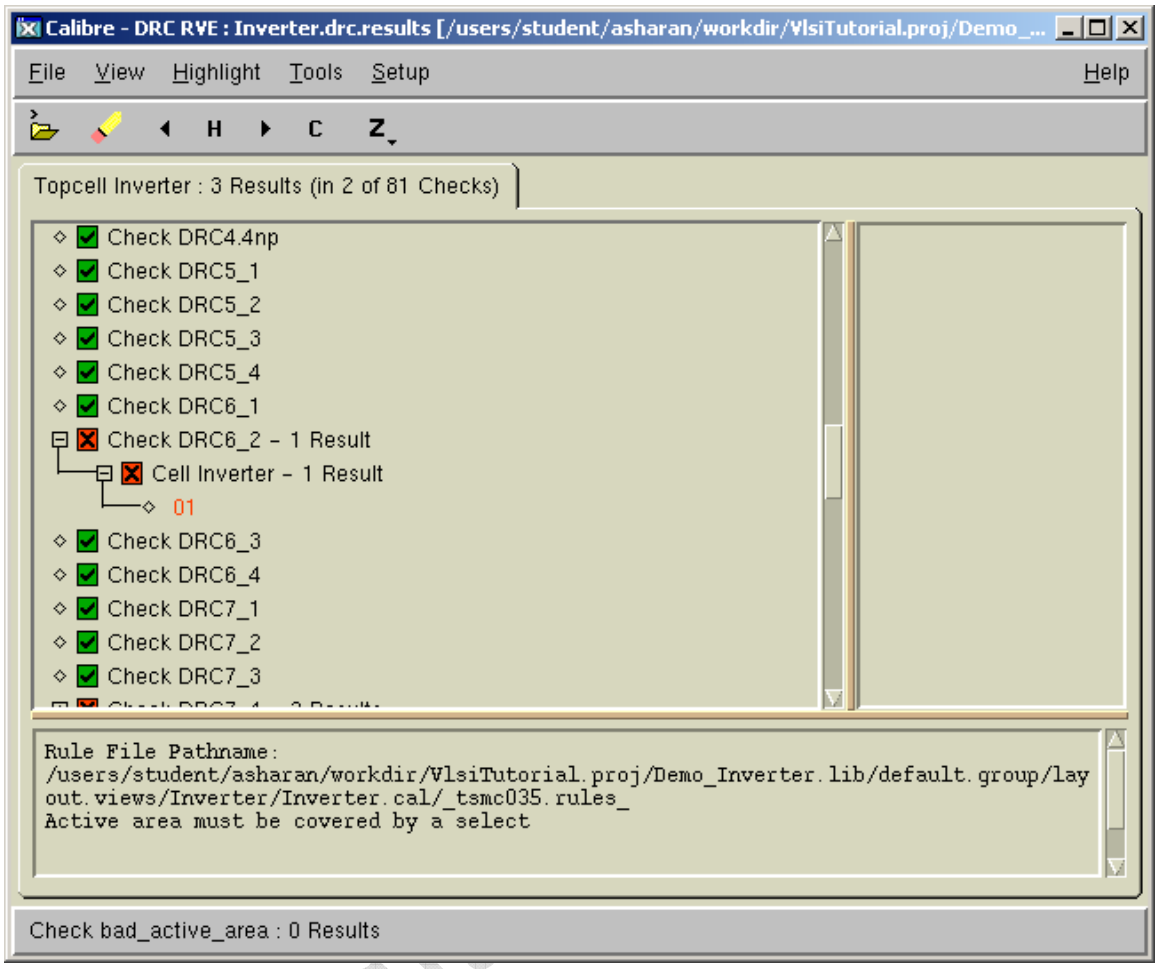


In case you have errors in your DRC the window would look as under. Click on the RED marked Squares and get to the errors. Correct them till you get No results

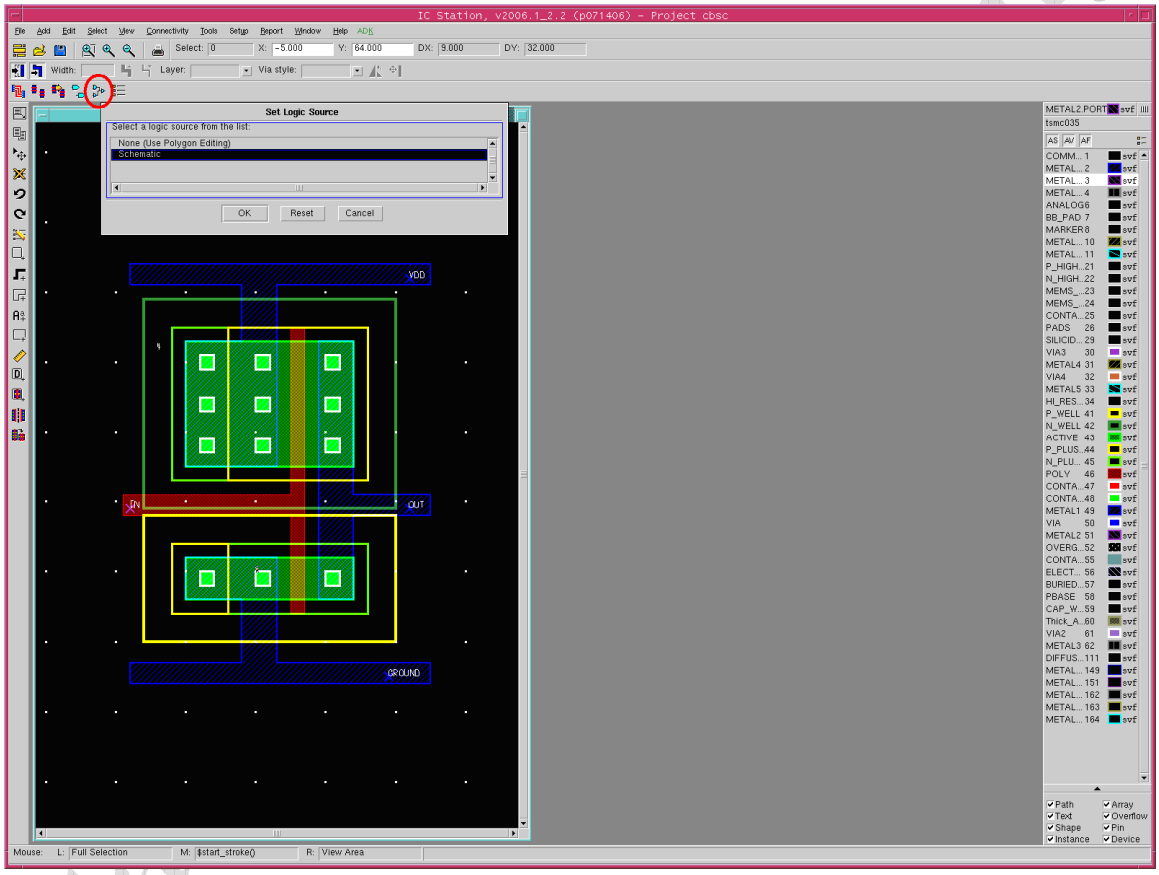




6. Verifying the Layout Vs Schematic (LVS)

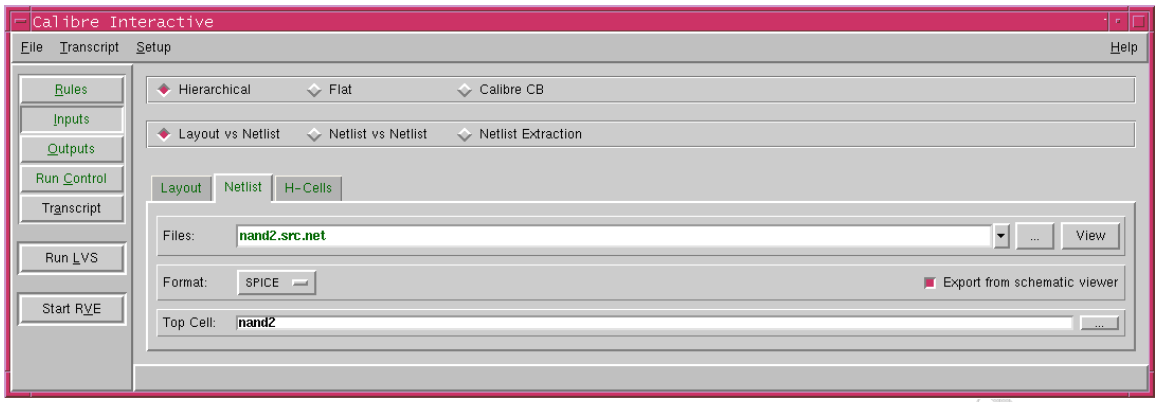
We first need to select the logic netlist for Calibre to compare with the layout we have drawn.

- Click **Tools > SDL/NDL**
- On the top toolbar, click the button for **Select Logic Source,** indicated below:
- Select **Schematic** as the Logic Source to use, as shown below:

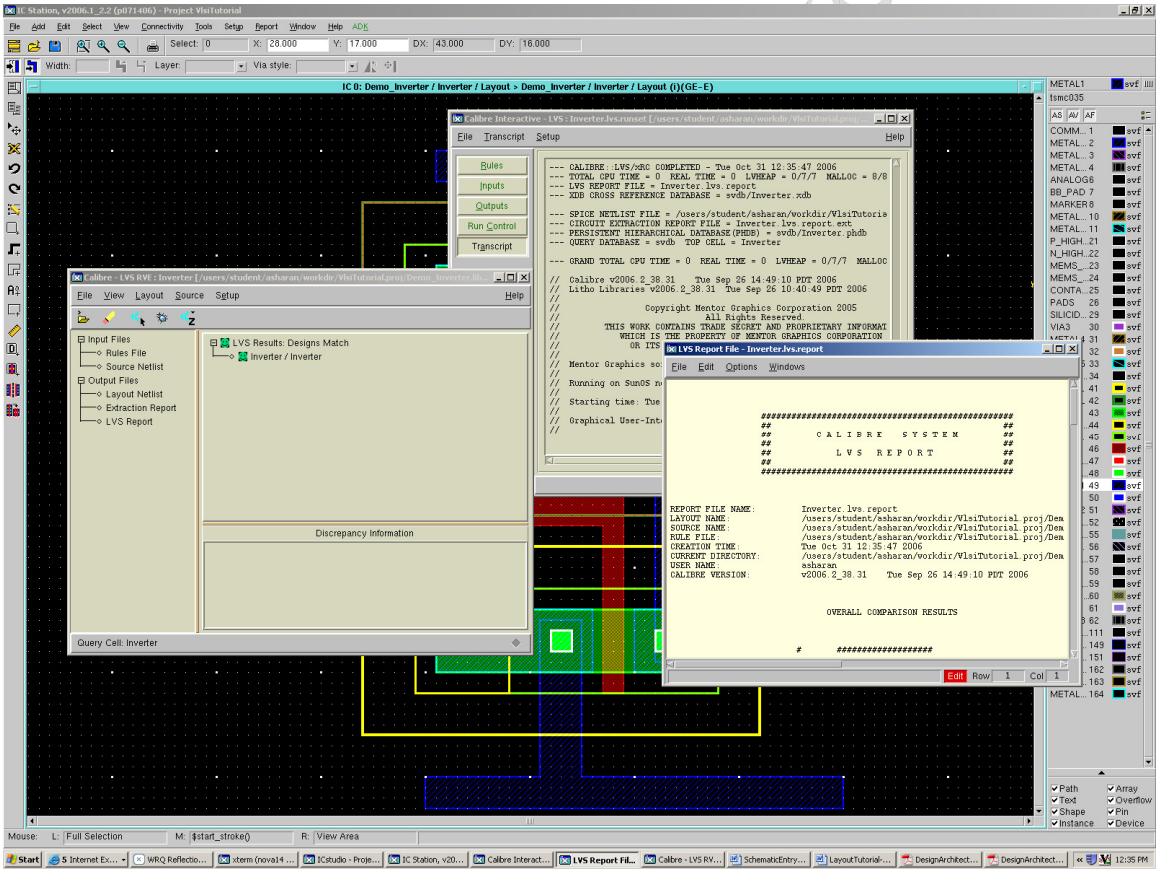


From the menu, select **Calibre > Run LVS**
In the window that pops up, enter the **Path to Calibre as:**
/opt/mentor-2008.1/adk3_1/technology/ic/process/tsmc035.calibre.rules

The LVS tool window will open:
Under **Inputs > Netlist**, check the box **Export from Schematic Viewer**



Click Run LVS to run the LVS Check:



If the Layout matches the source Netlist, the LVS Report will show a passing result. If there are errors, click on them in the RVE results window to get more information.

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