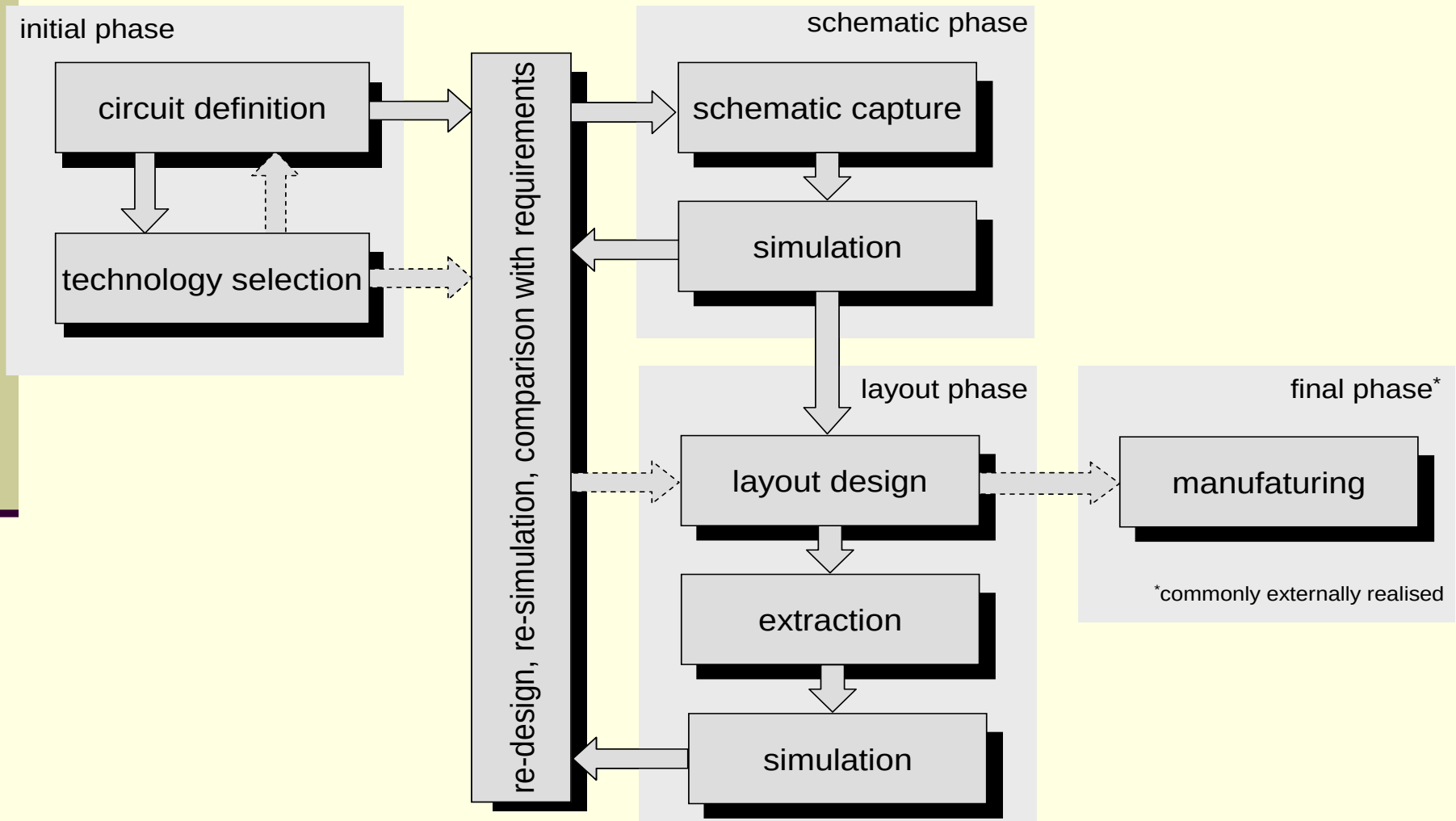
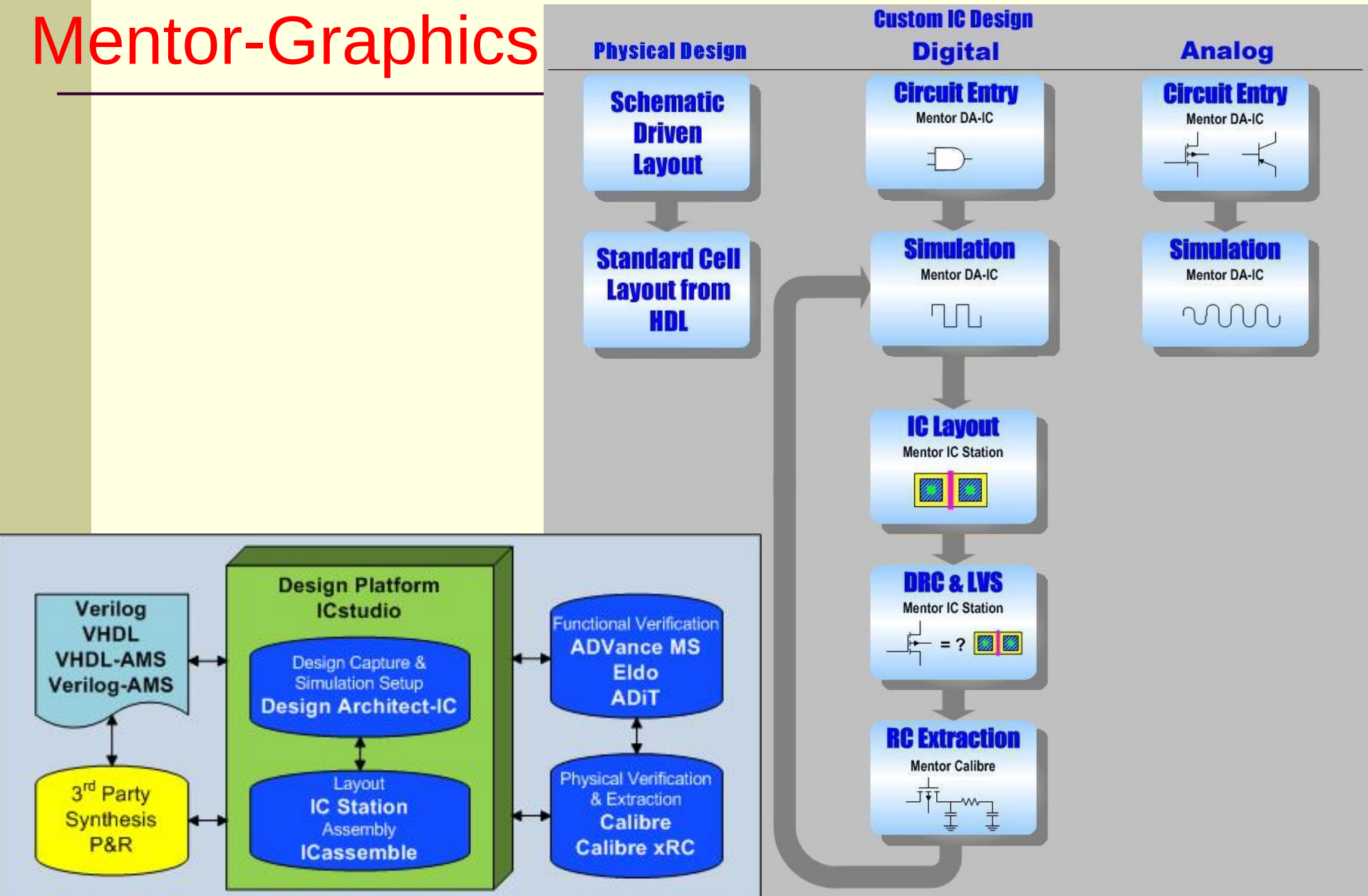
Návrhové prostredia v MG

Pavol Galajda, KEMT, FEI, TUKE
Pavol.Galajda@tuke.sk

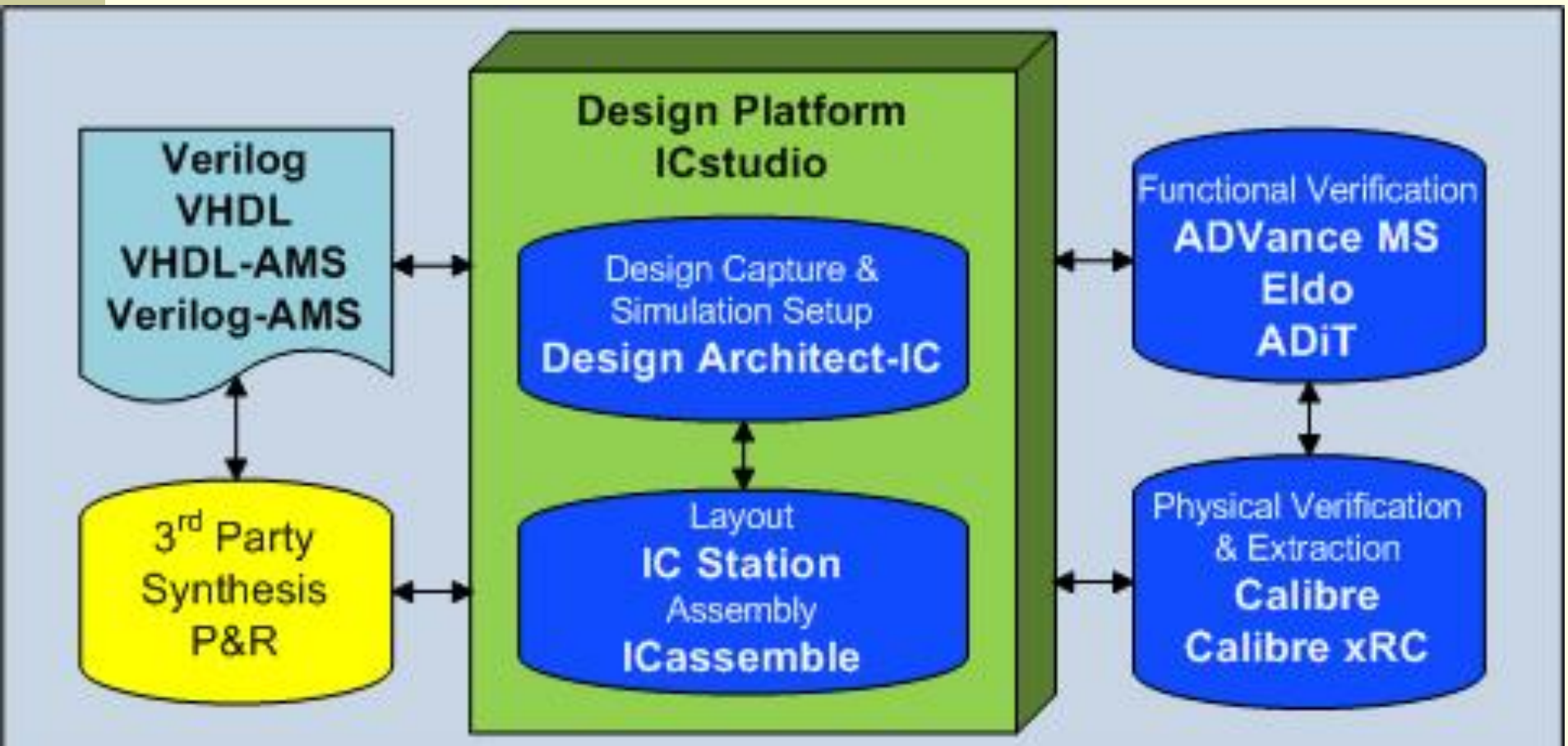
IC- postup pri návrhu



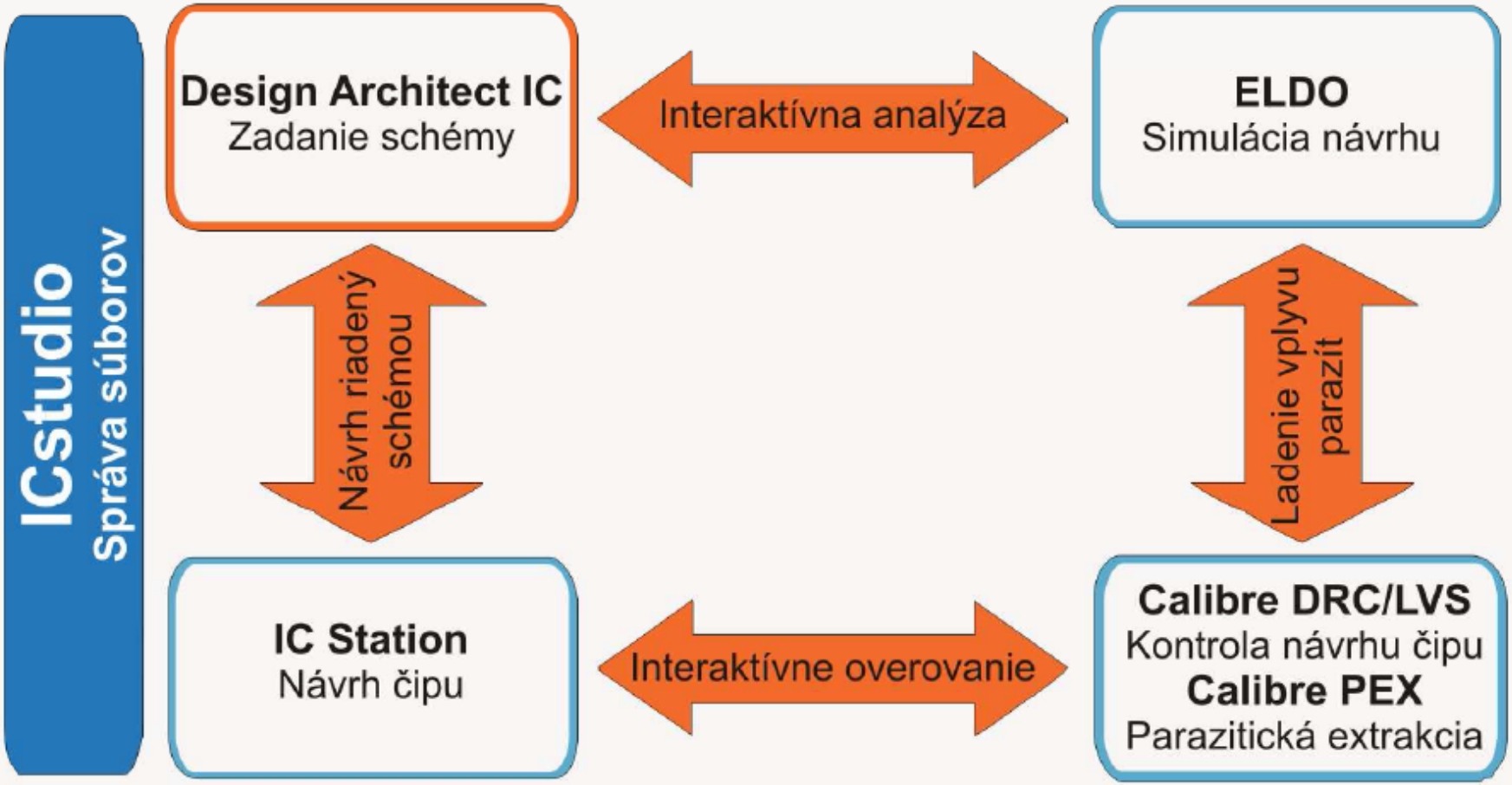
Postup pri návrhu prostredníctvom Mentor-Graphics



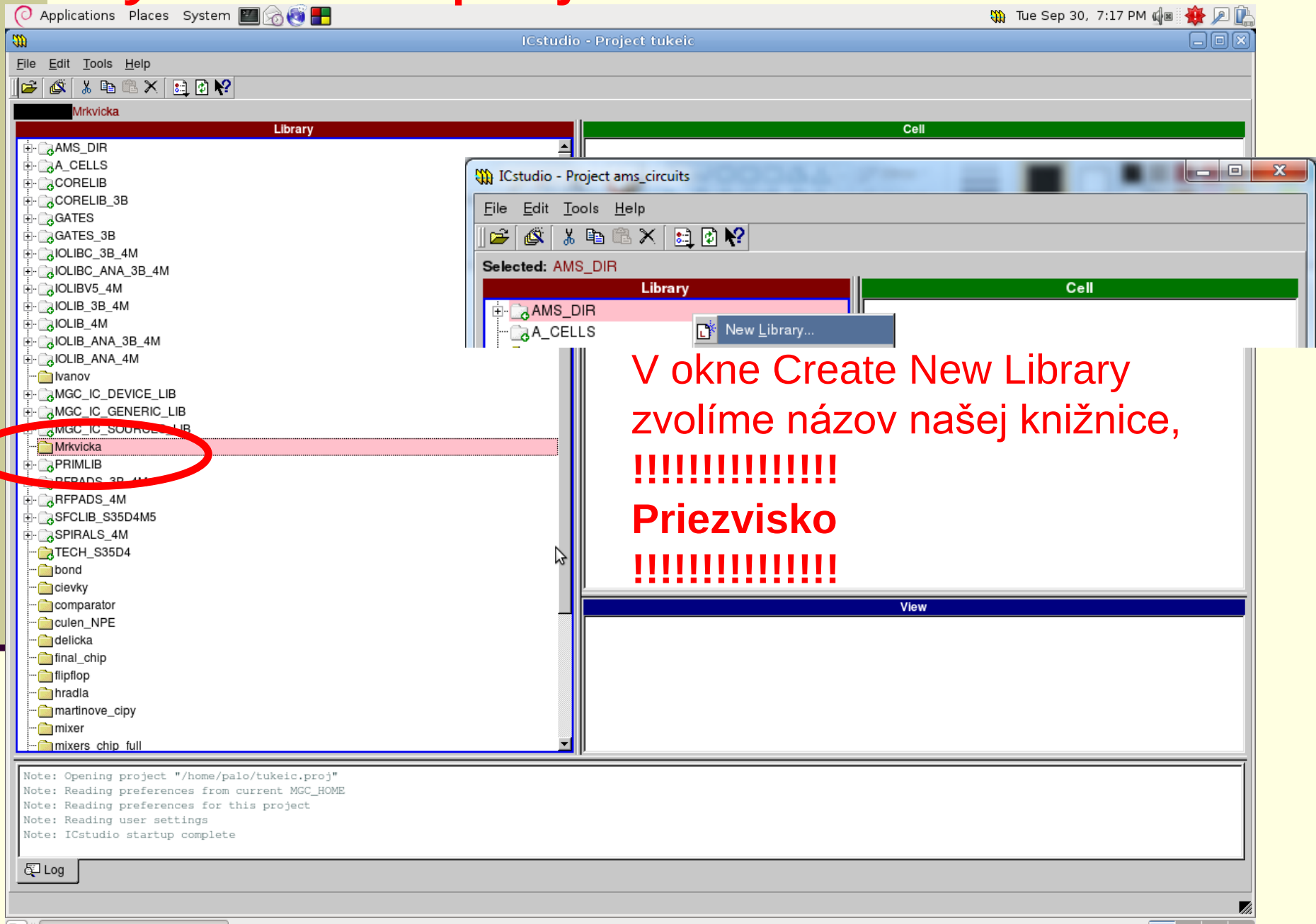
Postup pri návrhu prostredníctvom Mentor-Graphics



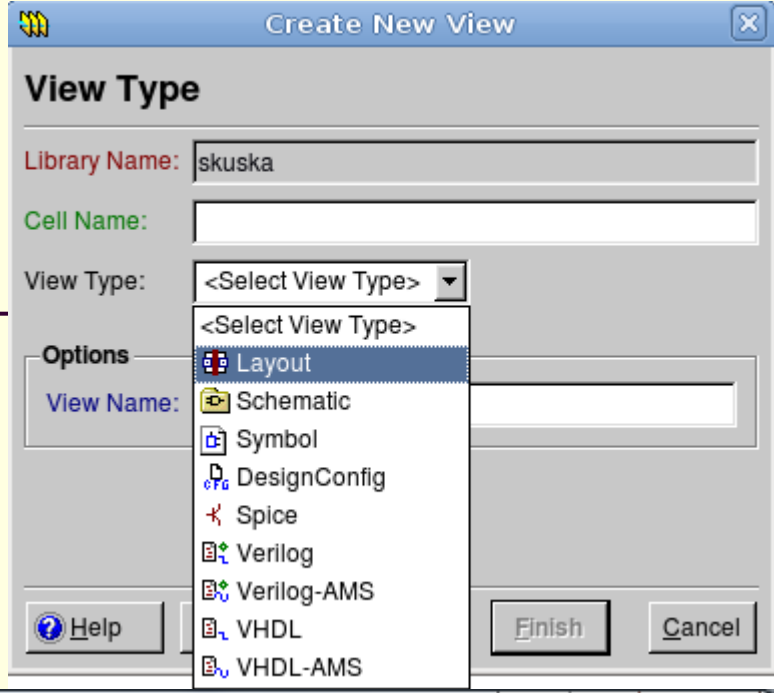
Kompletné riešenie návrhu IO od zadania schémy až po fyzický dizajn a overovanie obvodu

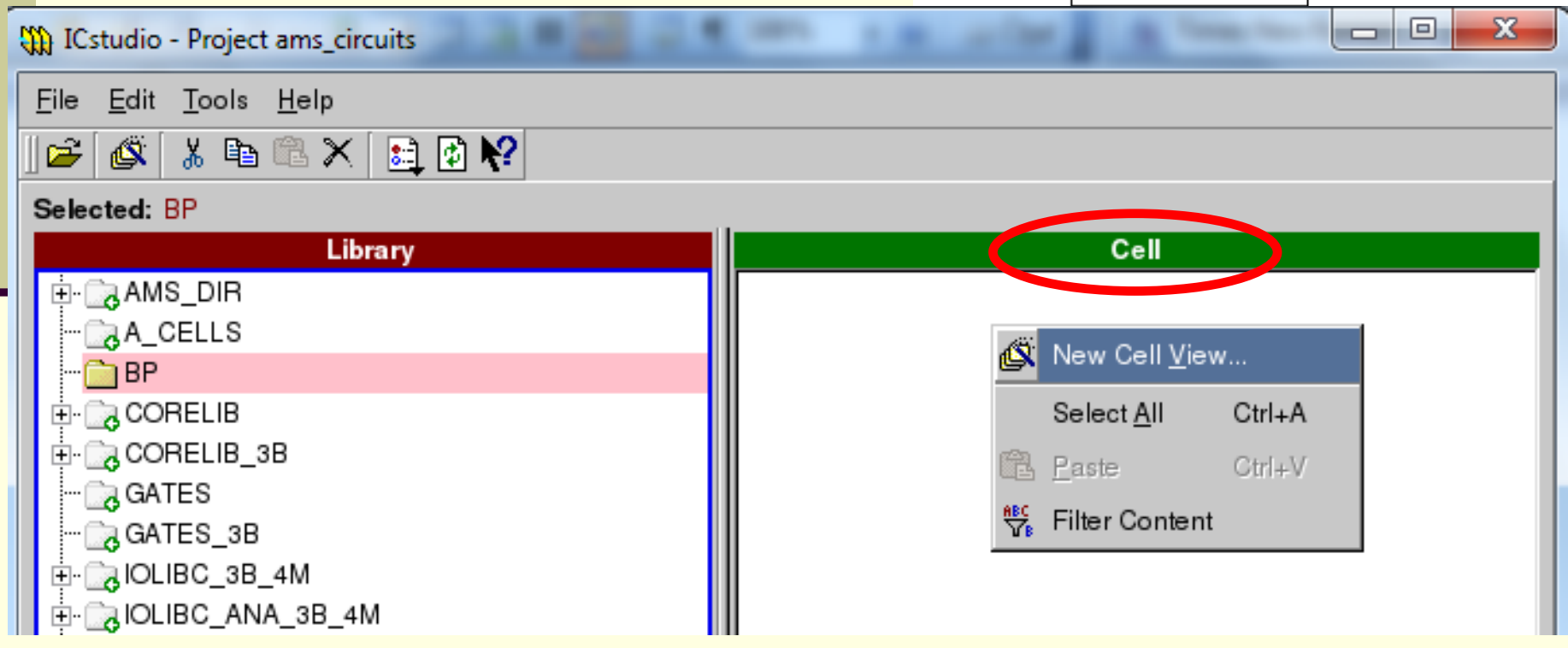


Vytvorenie projektu



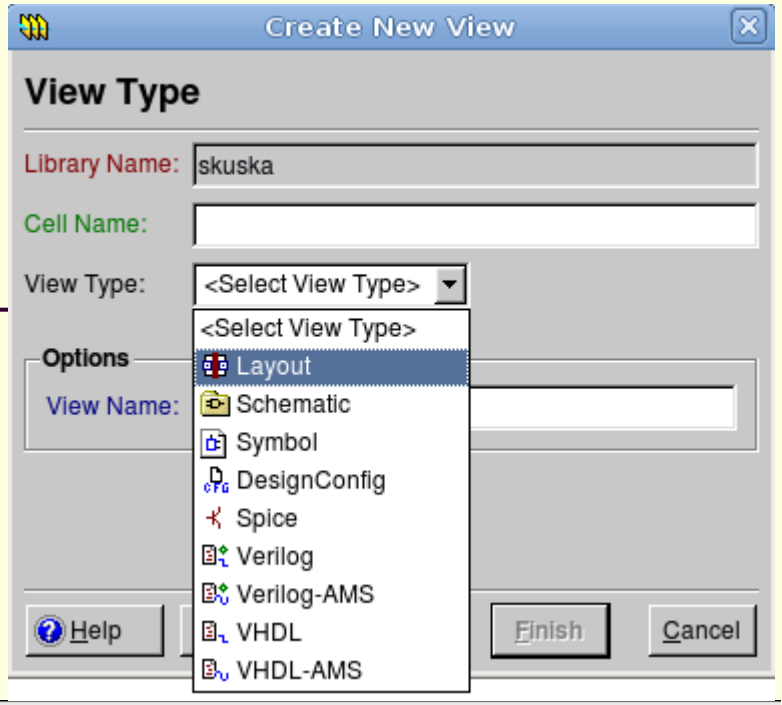
Vytvorenie bunky

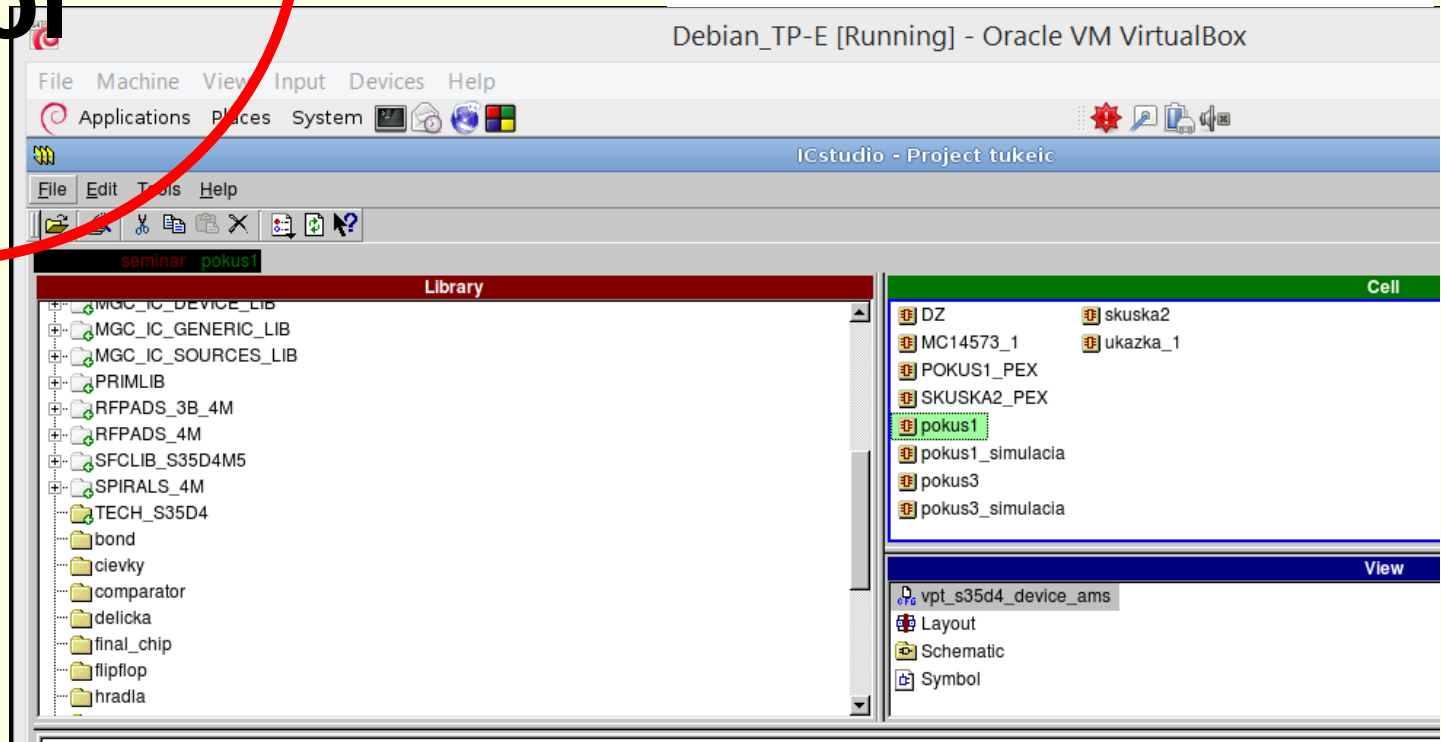




Vytvorenie bunky:

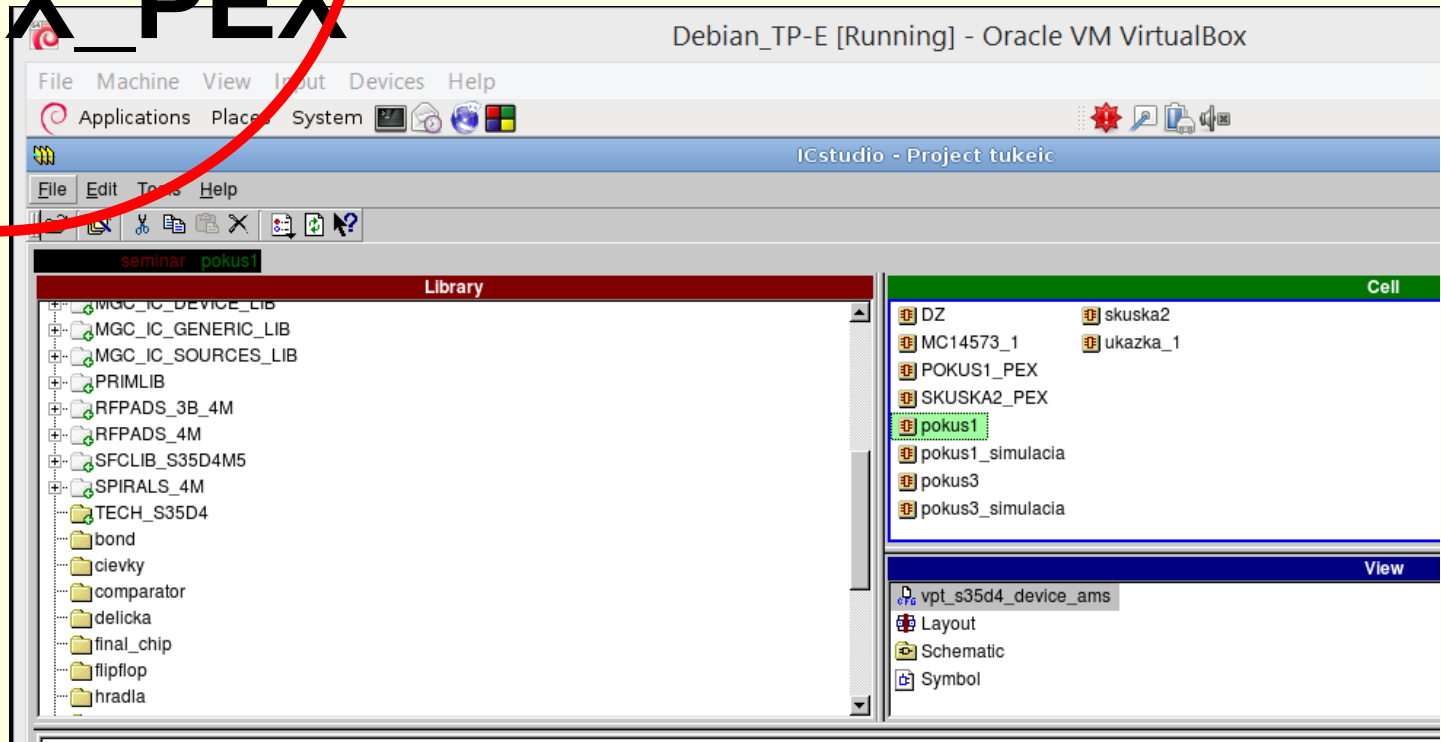
Schematic
Layout
Symbol
Spice



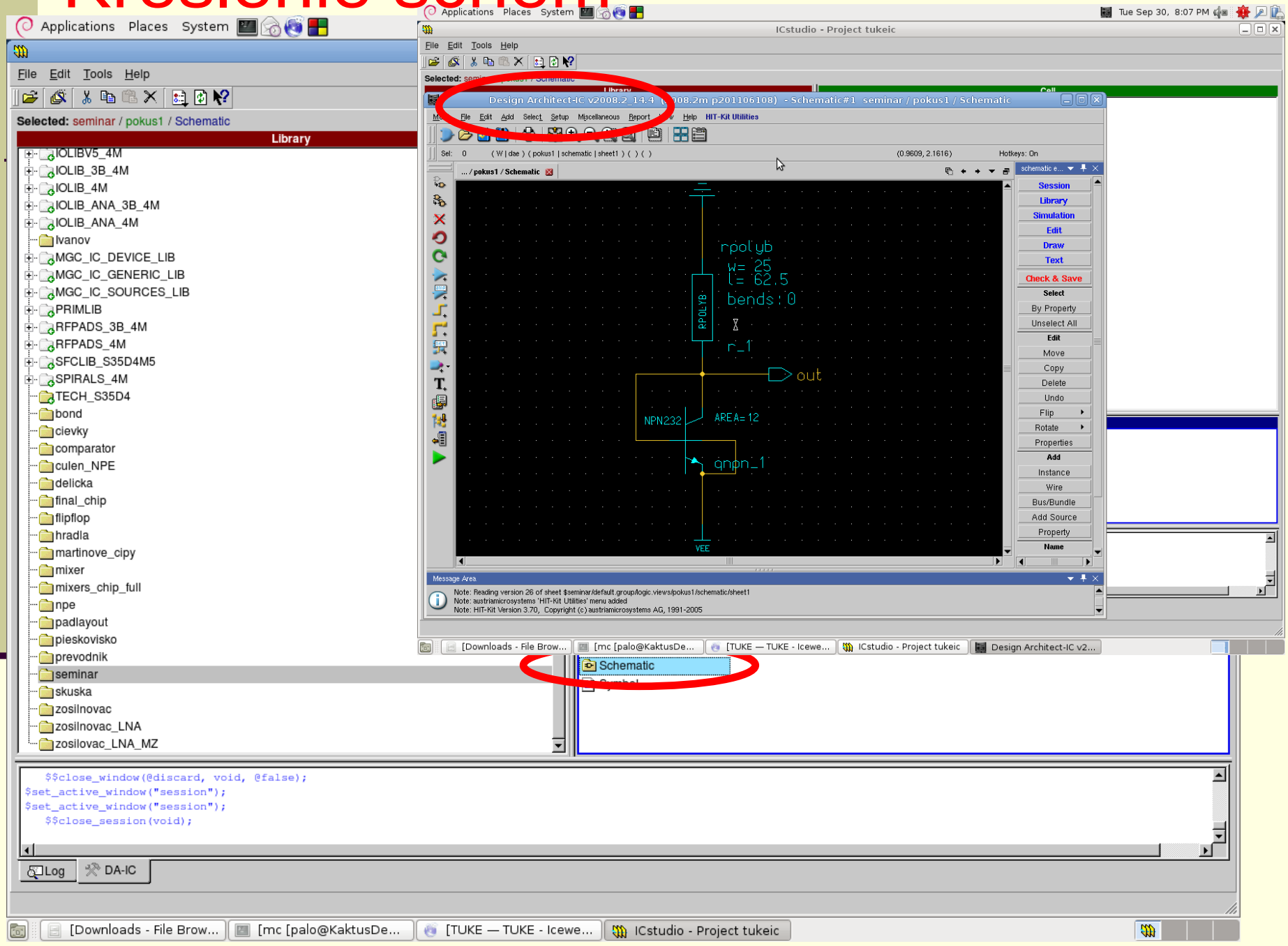


Vytvorenie bunky:

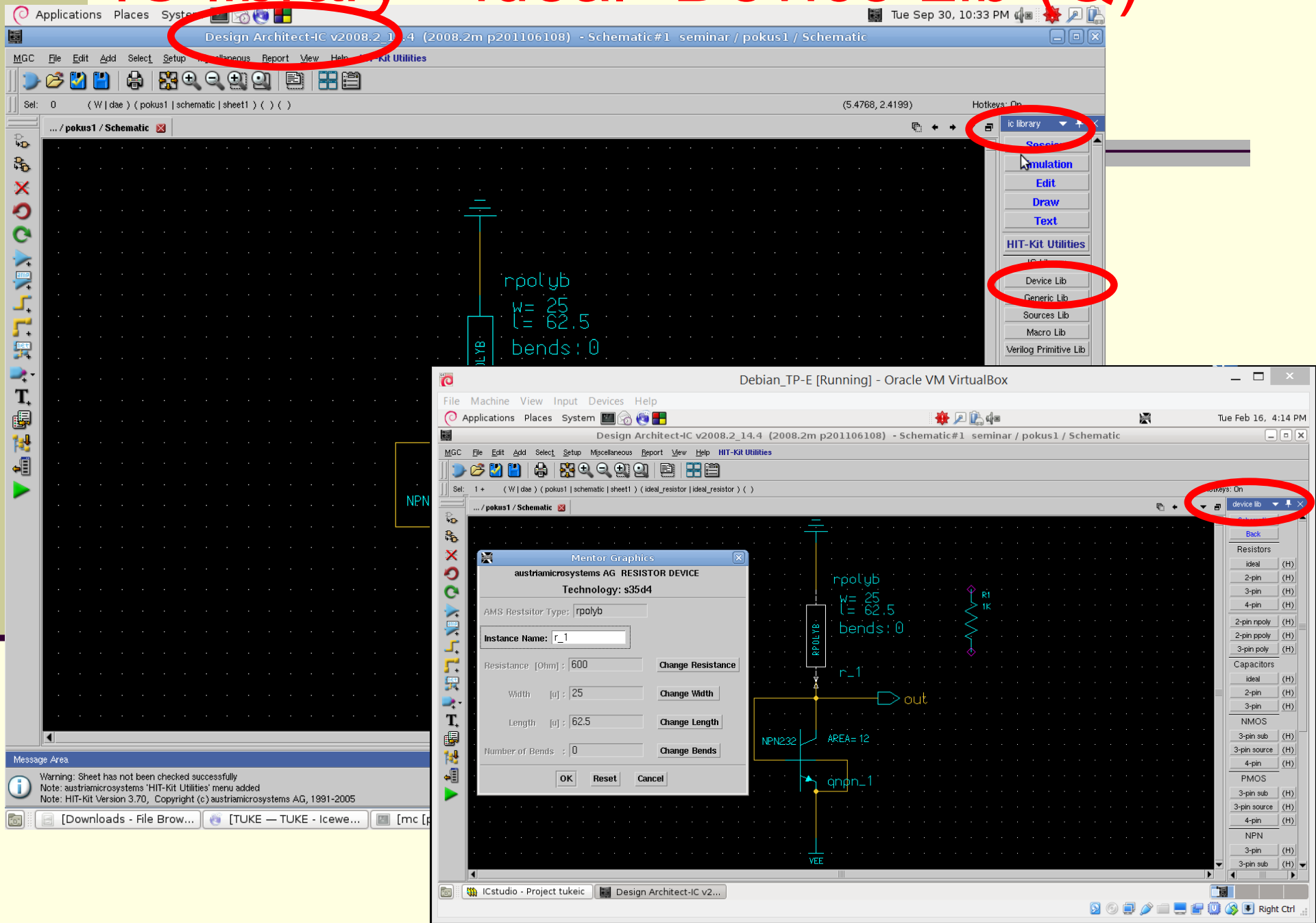
PokusX
PokusX_sim
PokusX_PEX



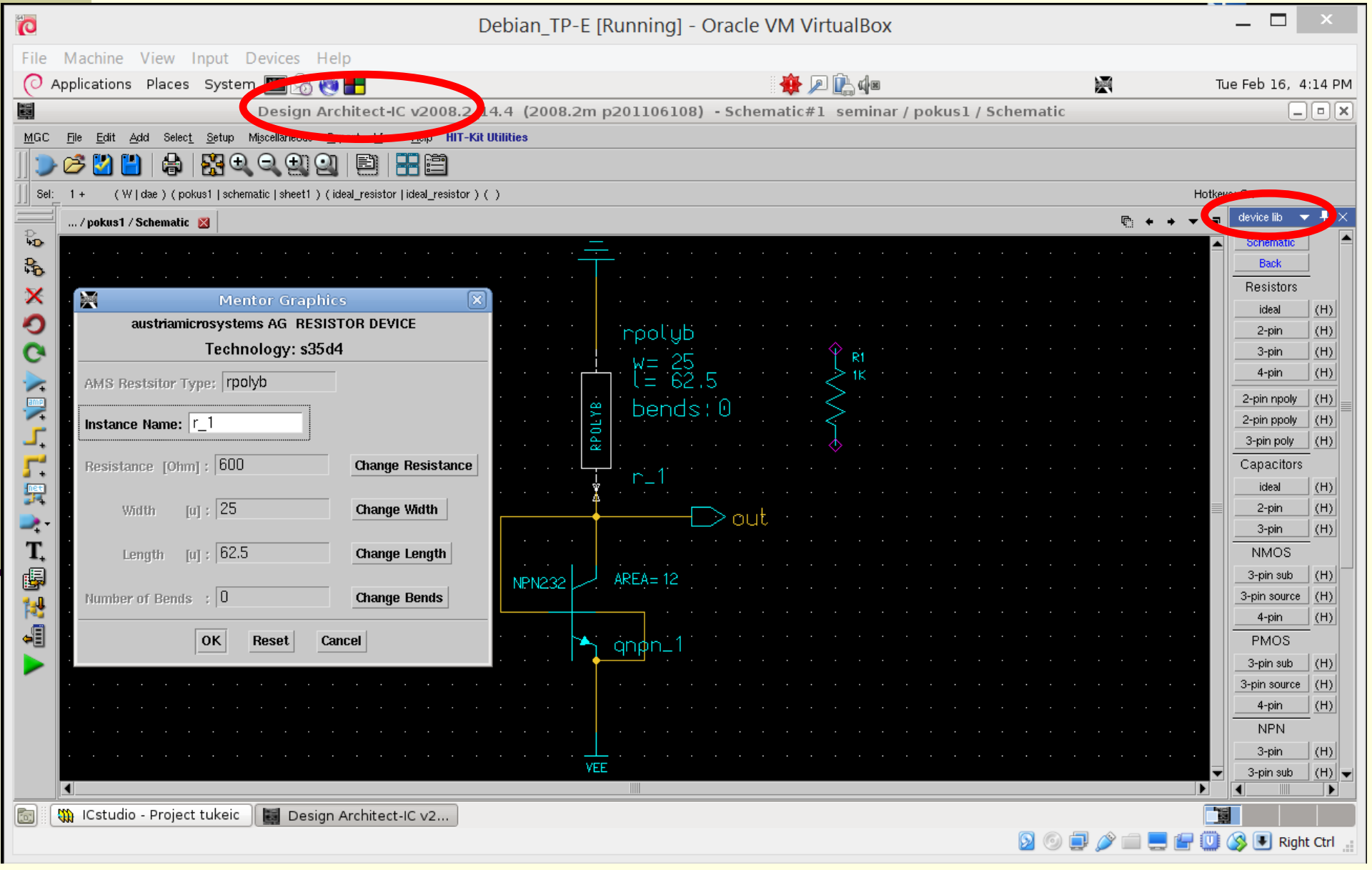
Kreslenie schém



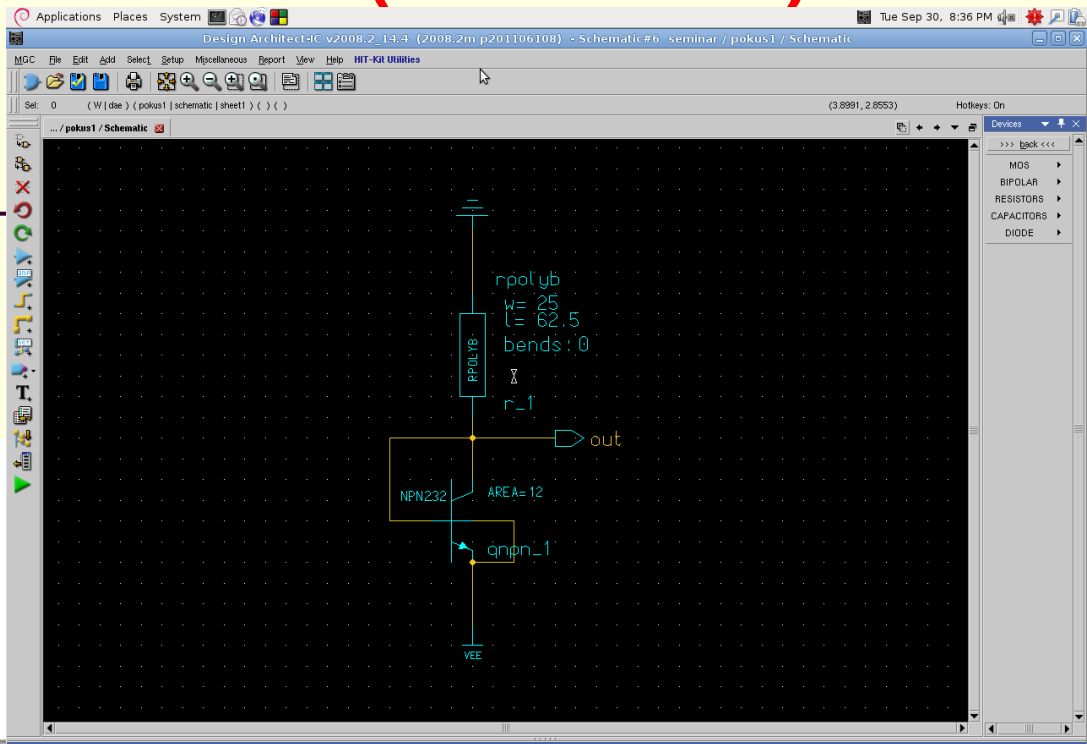
IC library- “ideal” Device Lib (Q)



IC library- “ideal” Device Lib (Q)

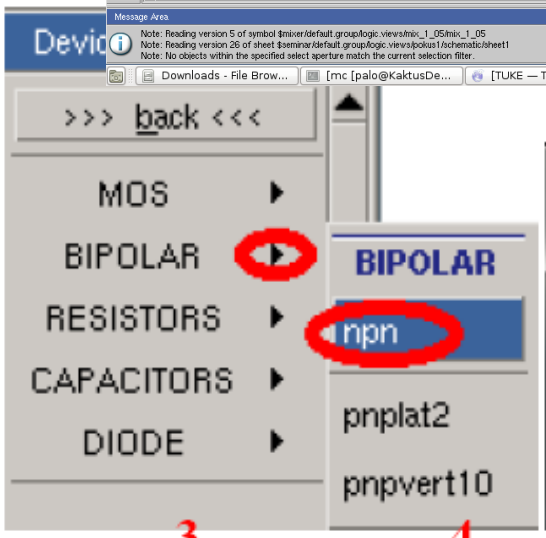


HIT-Kit Utilities- AMS (ALT+F6)

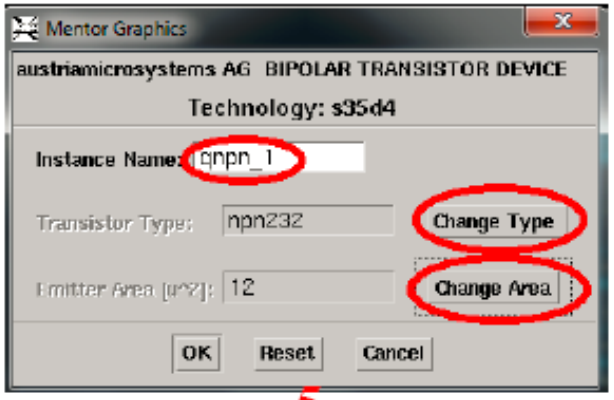


1.

2.

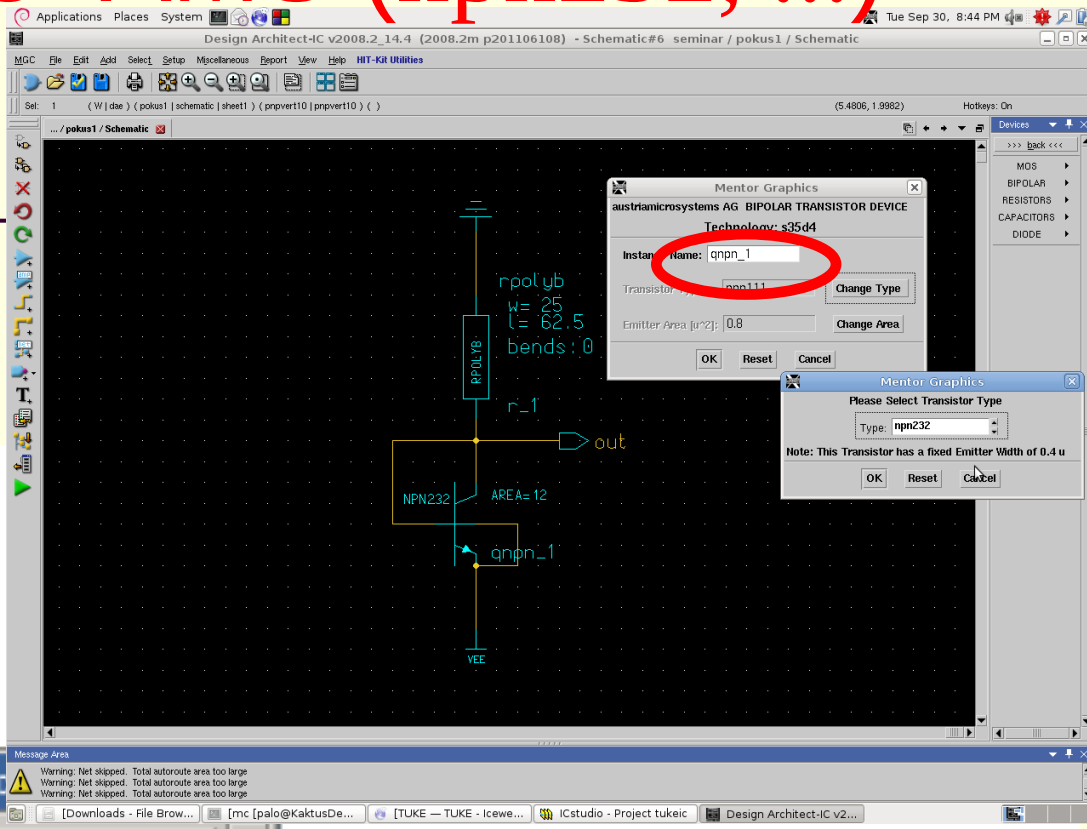


3. 4.



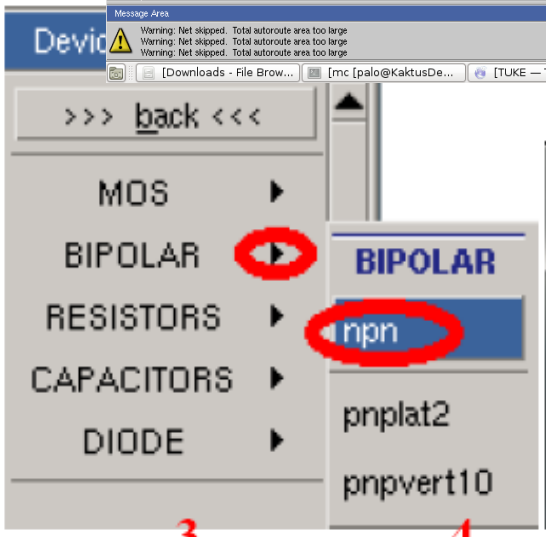
5.

HIT-Kit Utilities- AMS (npn232, ...)



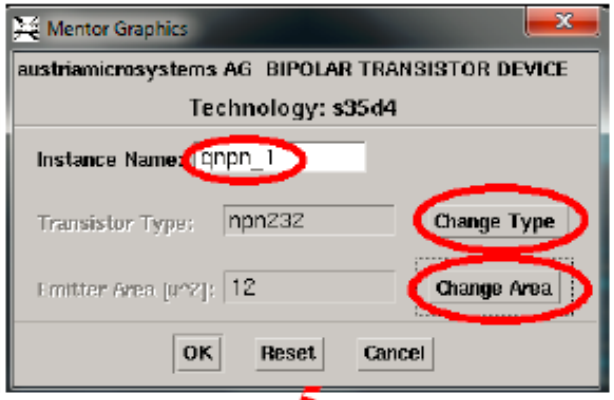
1.

2.



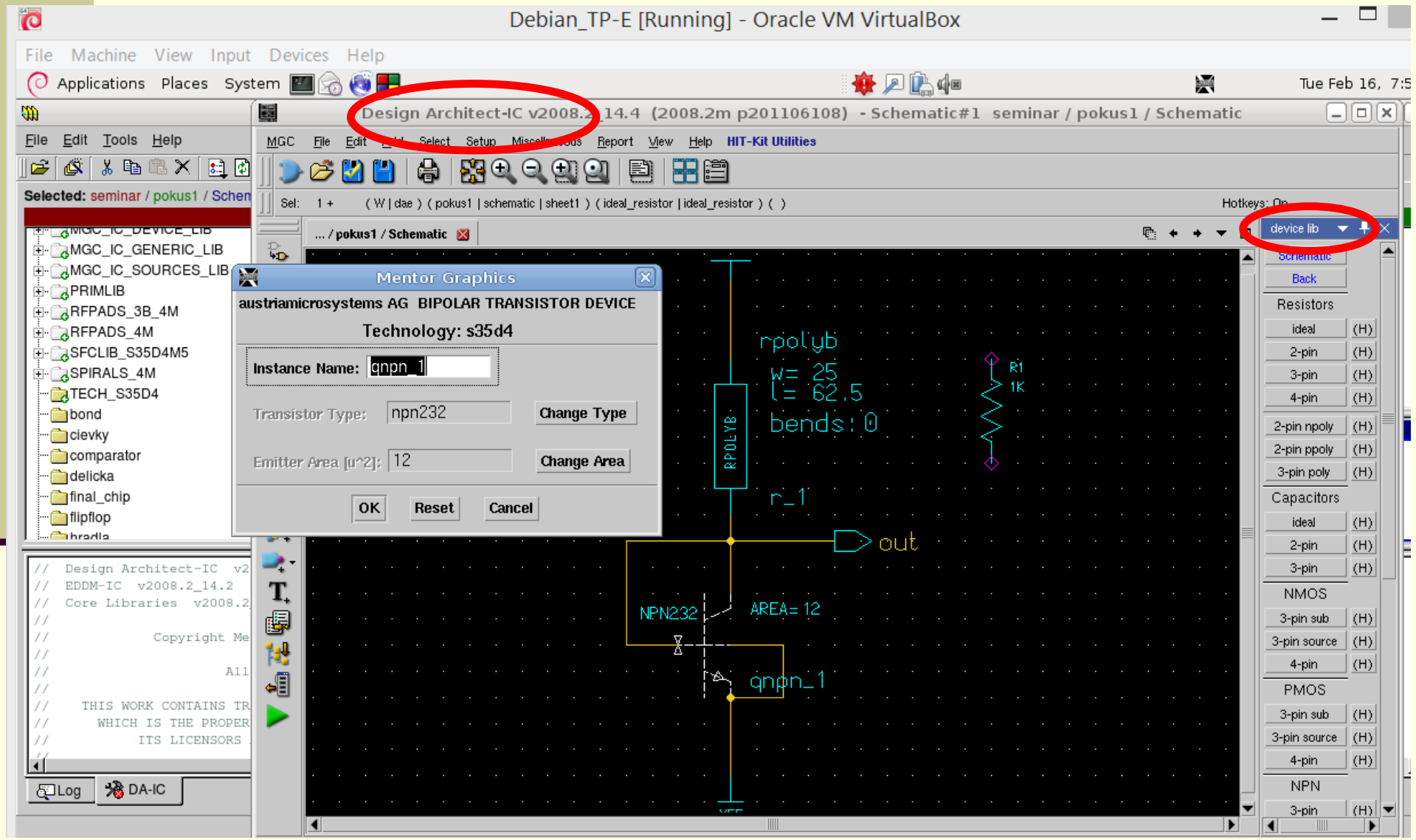
3.

4.



5.

HIT-Kit Utilities- AMS (ALT+F6)

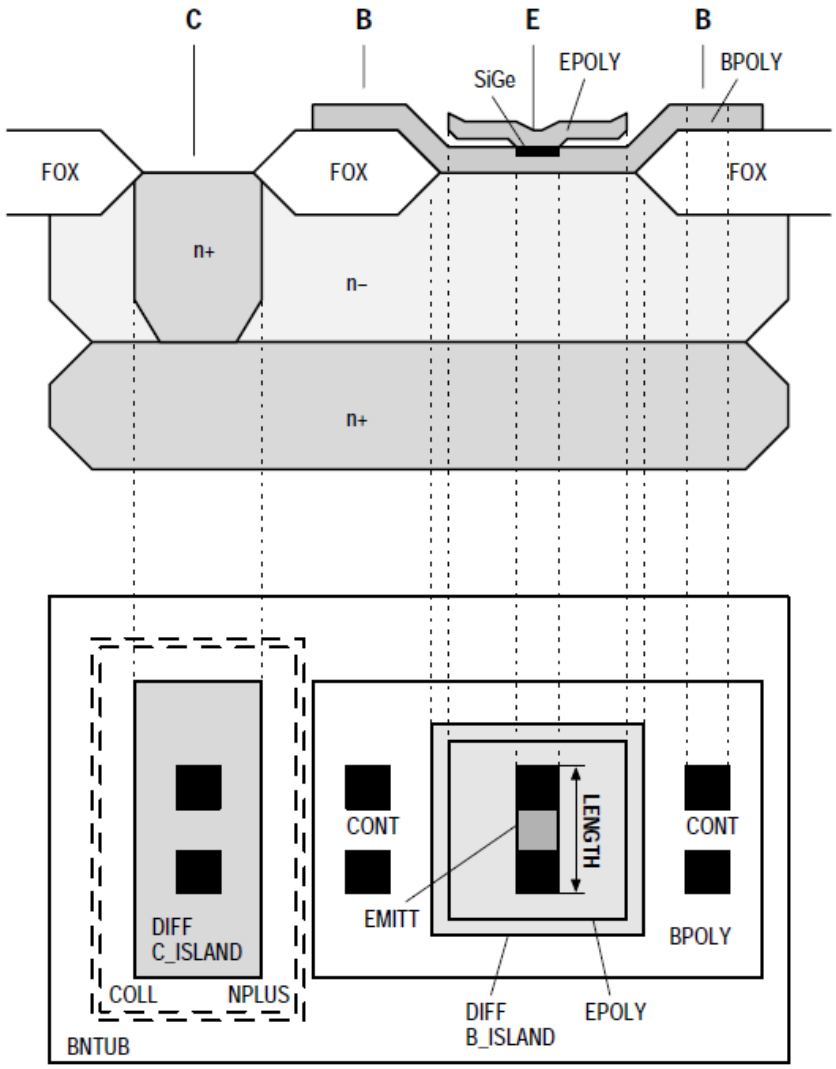


HIT-Kit Utilities- AMS

High Speed HBT

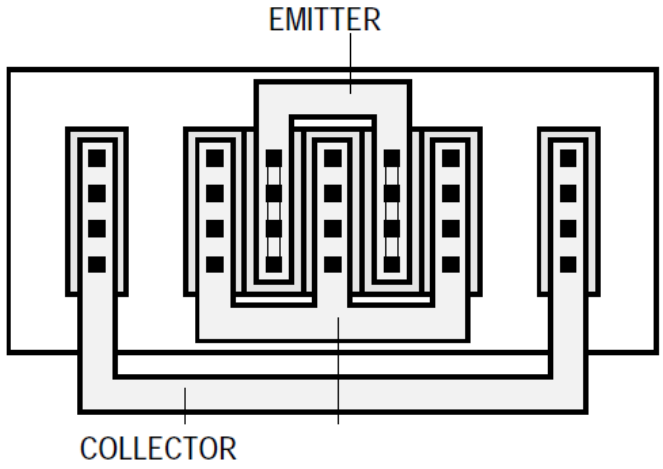
5.3.2 NPN121

Note: EMITTER LENGTH can be changed.
All BASE stripes must be connected to a single terminal.

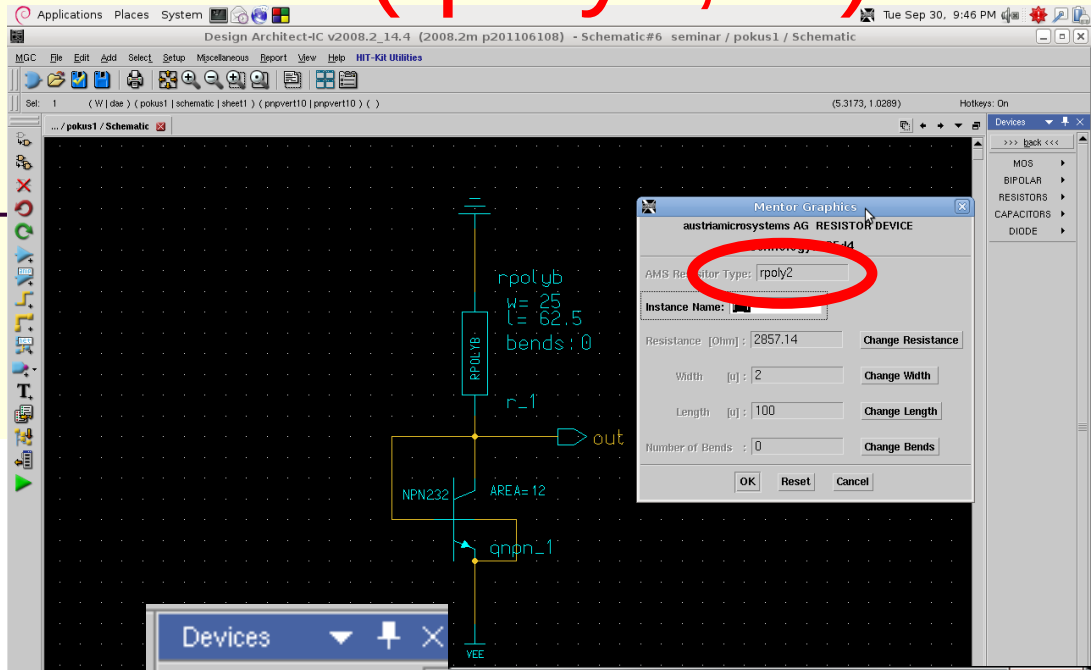


5.3.5 NPN232

Note: EMITTER LENGTH can be changed.
All COLLECTOR stripes must be connected to a single terminal.
All BASE stripes must be connected to a single terminal.
All EMITTER stripes must be connected to a single terminal.

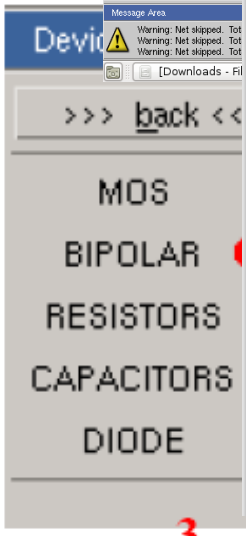


HIT-Kit Utilities- AMS (rpoly2, ...)

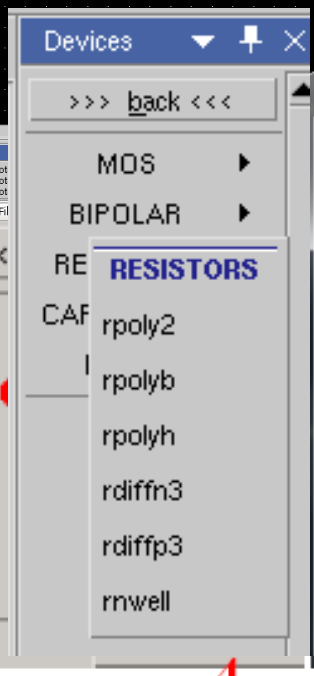


1.

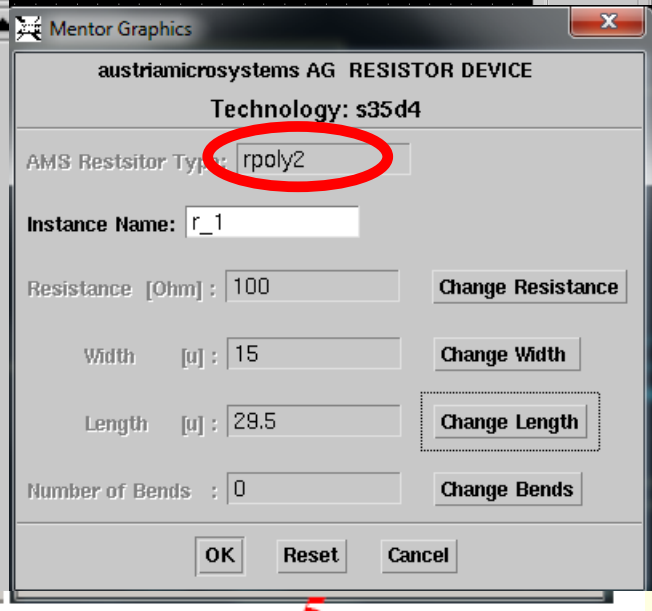
2.



3.

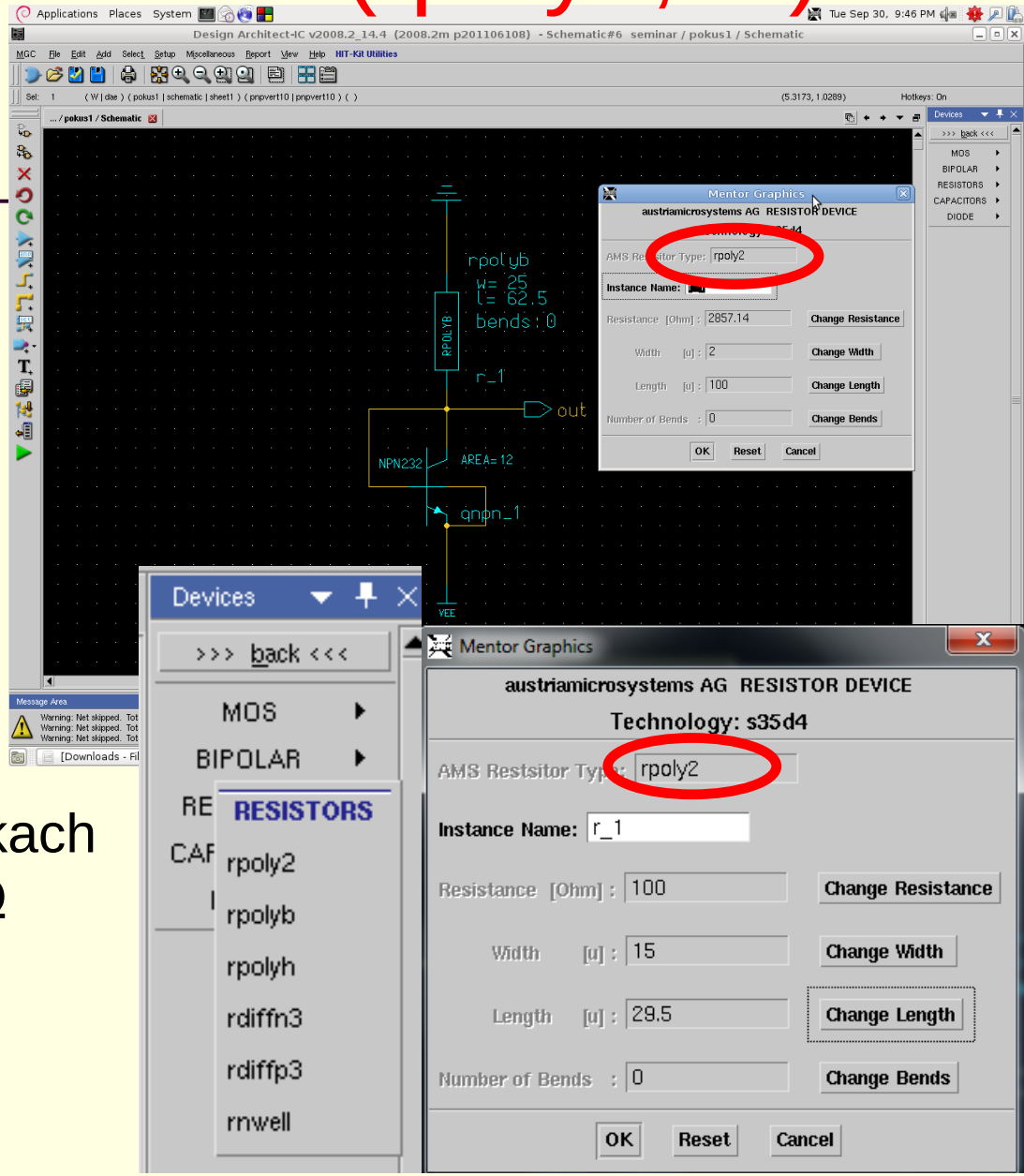


4.



5.

HIT-Kit Utilities- AMS (rpoly2, ...)

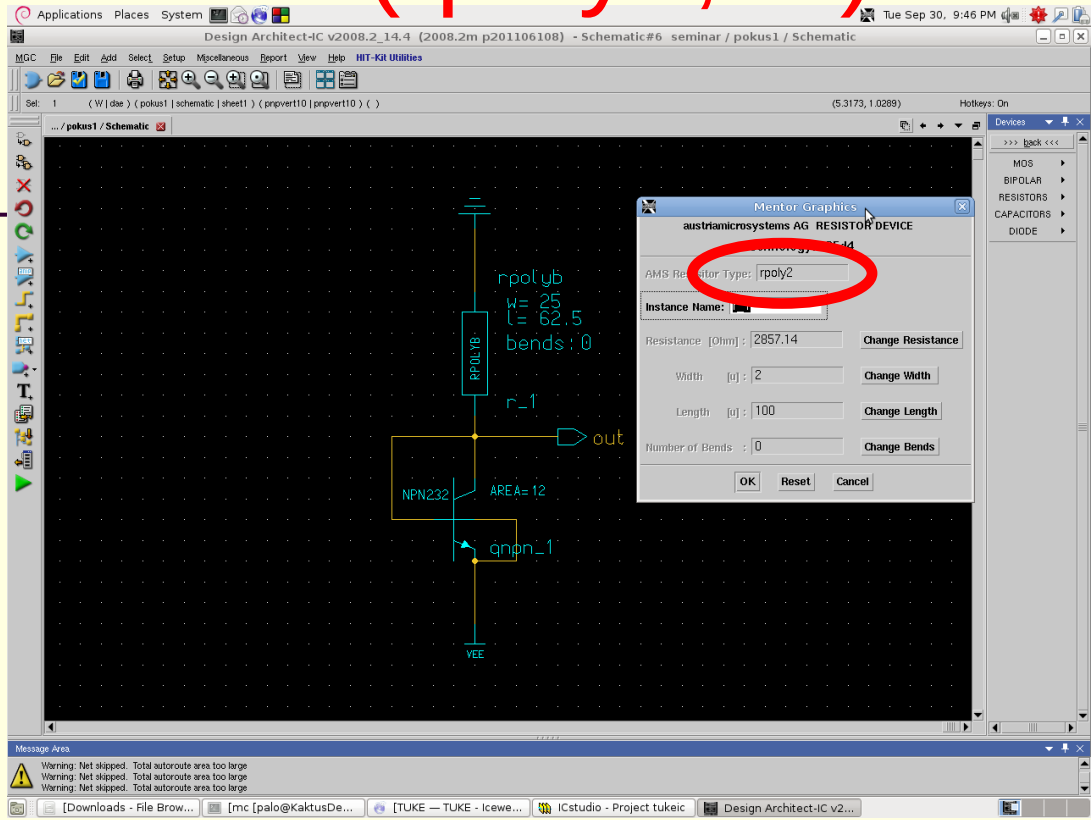


Hodnoty odporu v desiatkach až niekoľkých stovkách Ω
Rpoly2

Pre vyššie hodnoty
Rpolyb a Rpolyh

HIT-Kit Utilities- AMS (rpoly2, ...)

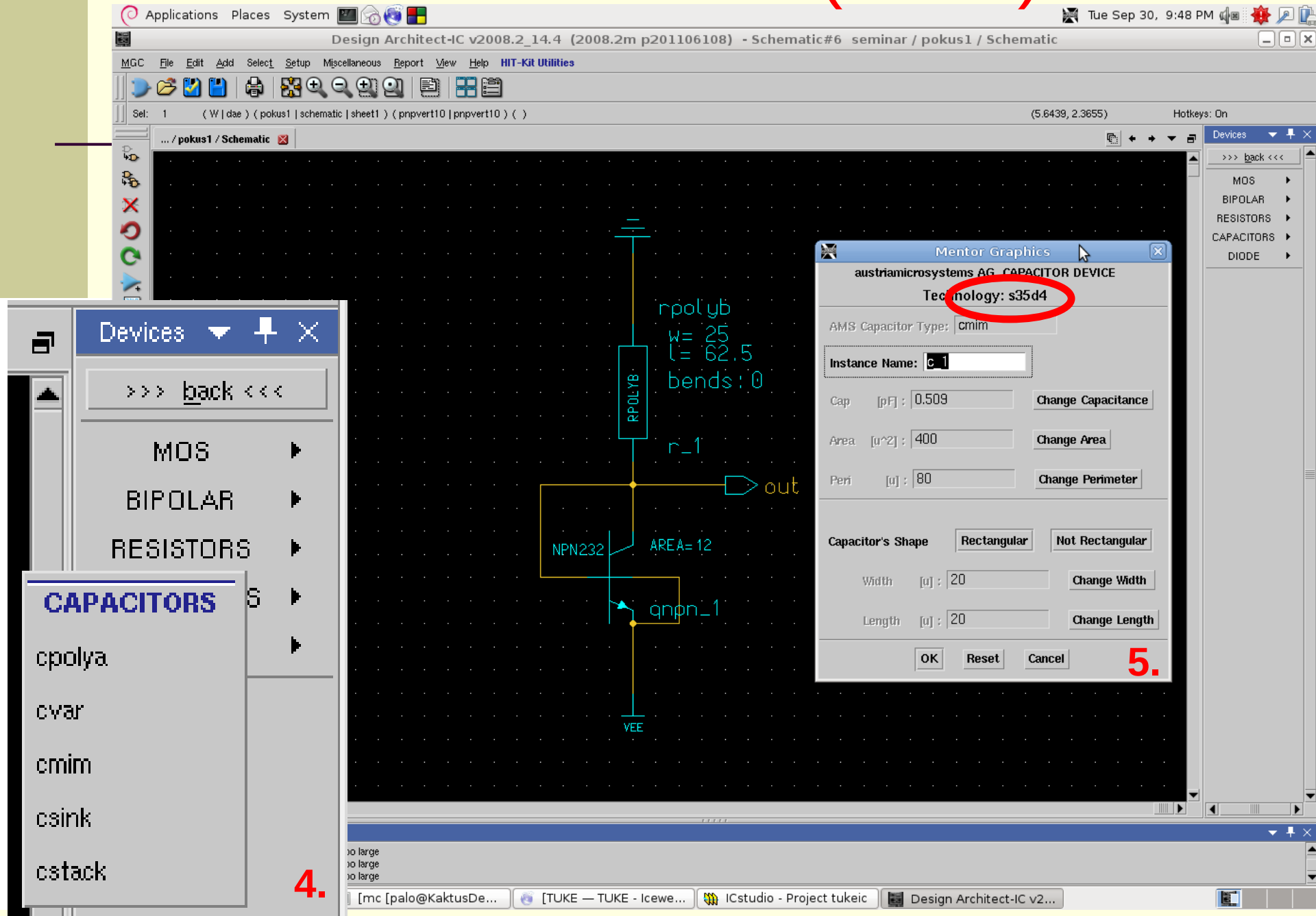
Dĺžka rezistora je úmerná jeho odporu, pričom je potrebné podľa rezistivity a dovolenej prúdovej hustoty odporovej vrstvy zvoliť vhodný typ rezistora pre danú hodnotu a prúd tak, aby mal **prípustné rozmery**.



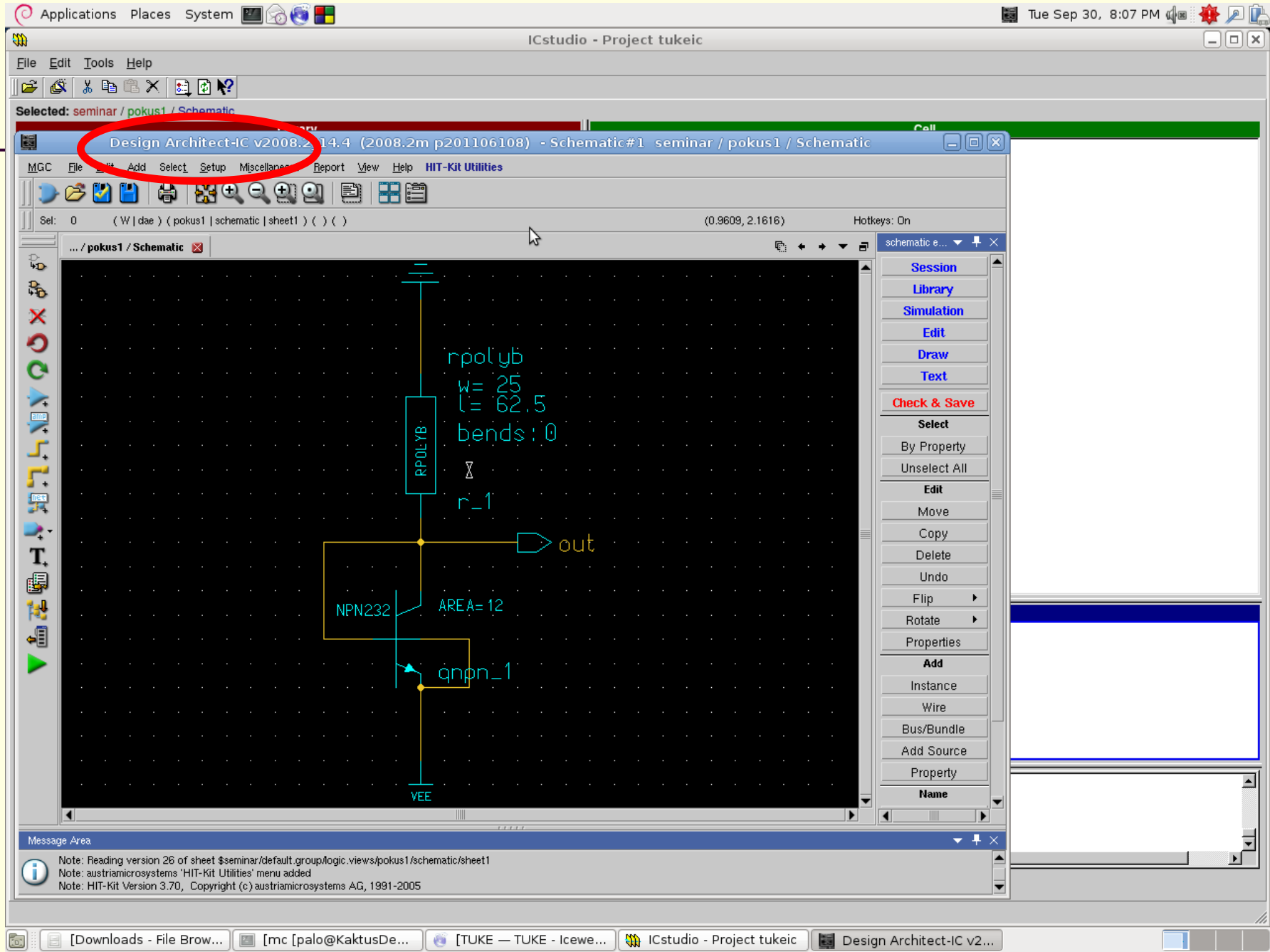
Väčšinu plochy čipu zaberajú rezistory, ktorých šírka musí rovnako ako šírka vodivých spojov s dostatočnou rezervou **zodpovedať maximálnej prúdovej hustote danej vrstvy** určenej výrobcom.

Niekedy je vhodné rezistor rozdeliť na dva paralelné rezistory dvojnásobného odporu, pretože výrobca neodporúča rozmery rezistorov, kde šírka je väčšia ako dĺžka.

HIT-Kit Utilities- AMS (cmim)



Kreslenie schém- F3= Add Wire



Porty

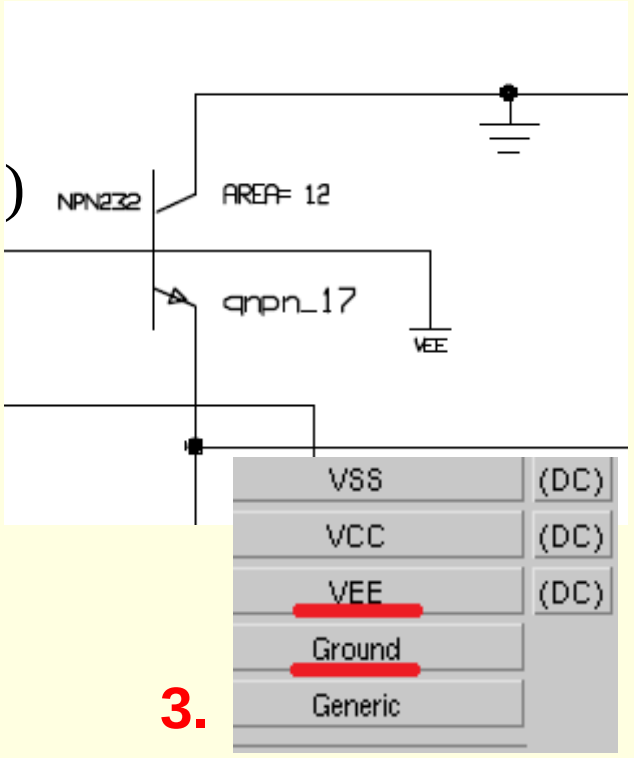
Port *VEE*, nájdeme v ponuke *Generic Library → VEE*.
Slúži ako odkaz pre ostatné porty *VEE*, aby bol návrh prehľadnejší.

Z *AMS Library* pomocou *MGC Library* spať do *IC library*.
kde je *Generic Library*.

Nájdeme tu aj „zem“ *Ground* = 0V (ref. pot.)

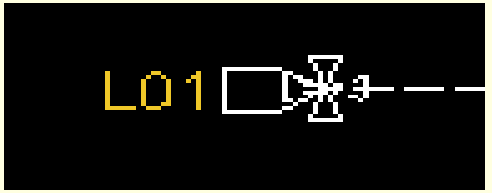
1.

2.



3.

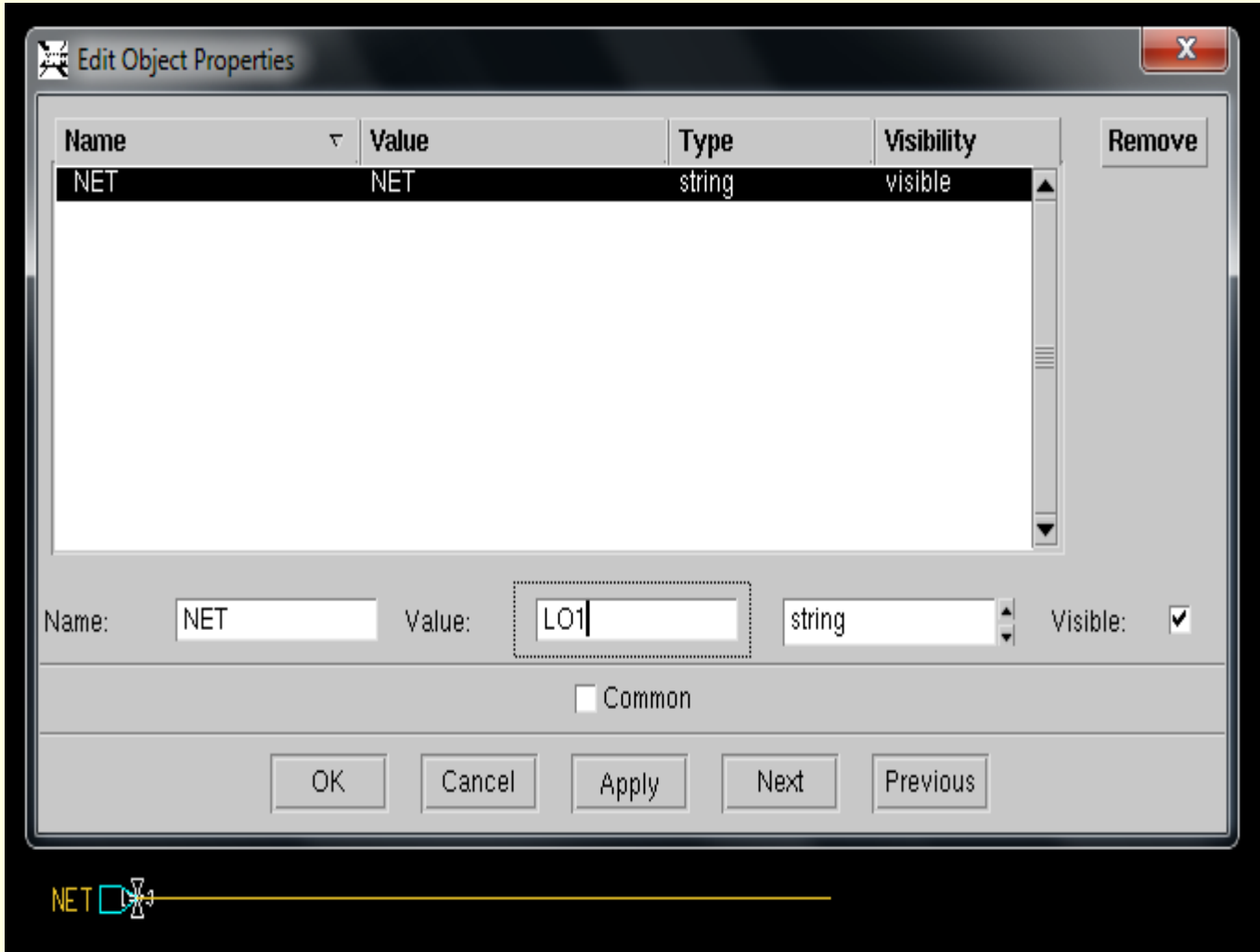
Porty- Vloženie portov



Ľavá lišta

1.

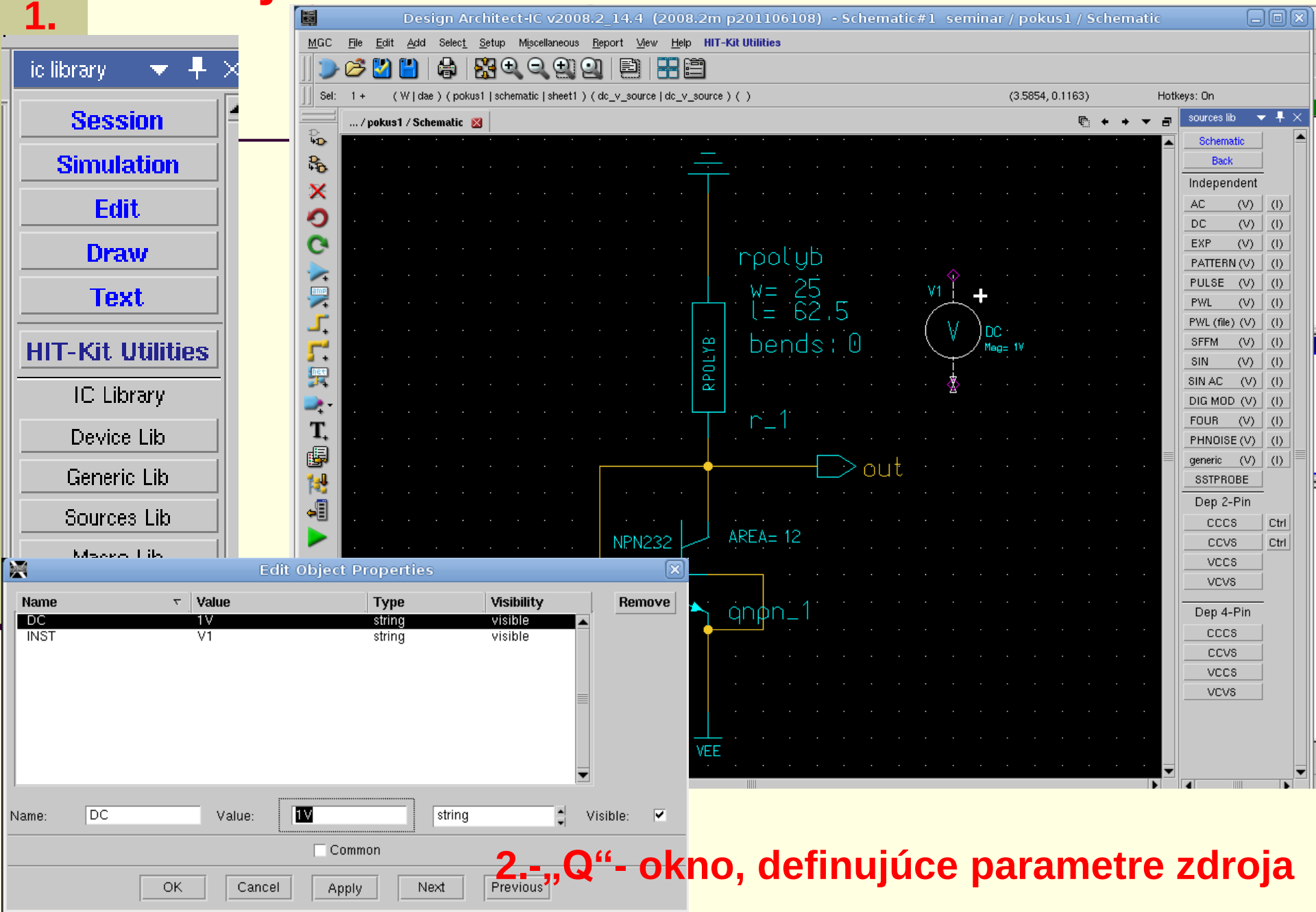
2. - „Q“



Zdroje

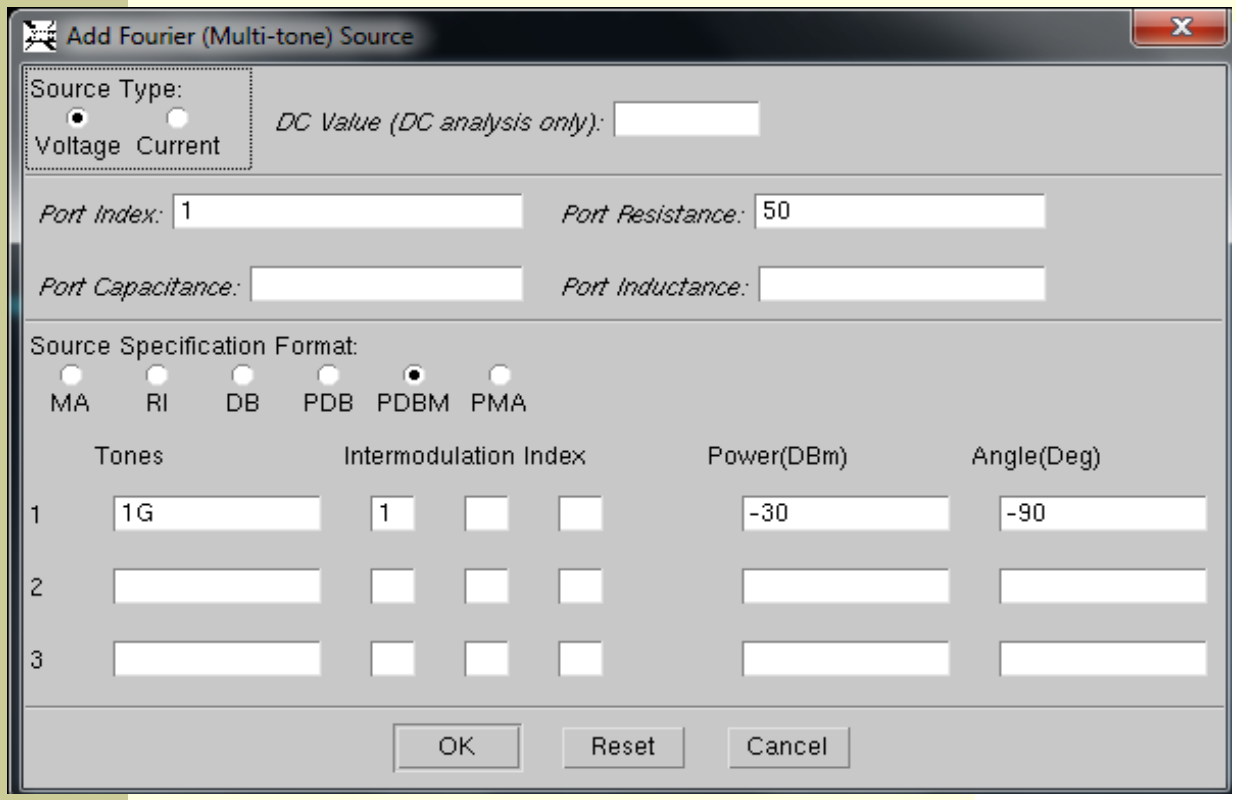
V *IC Library* vyberieme *Sources Library* → *DC (V)*

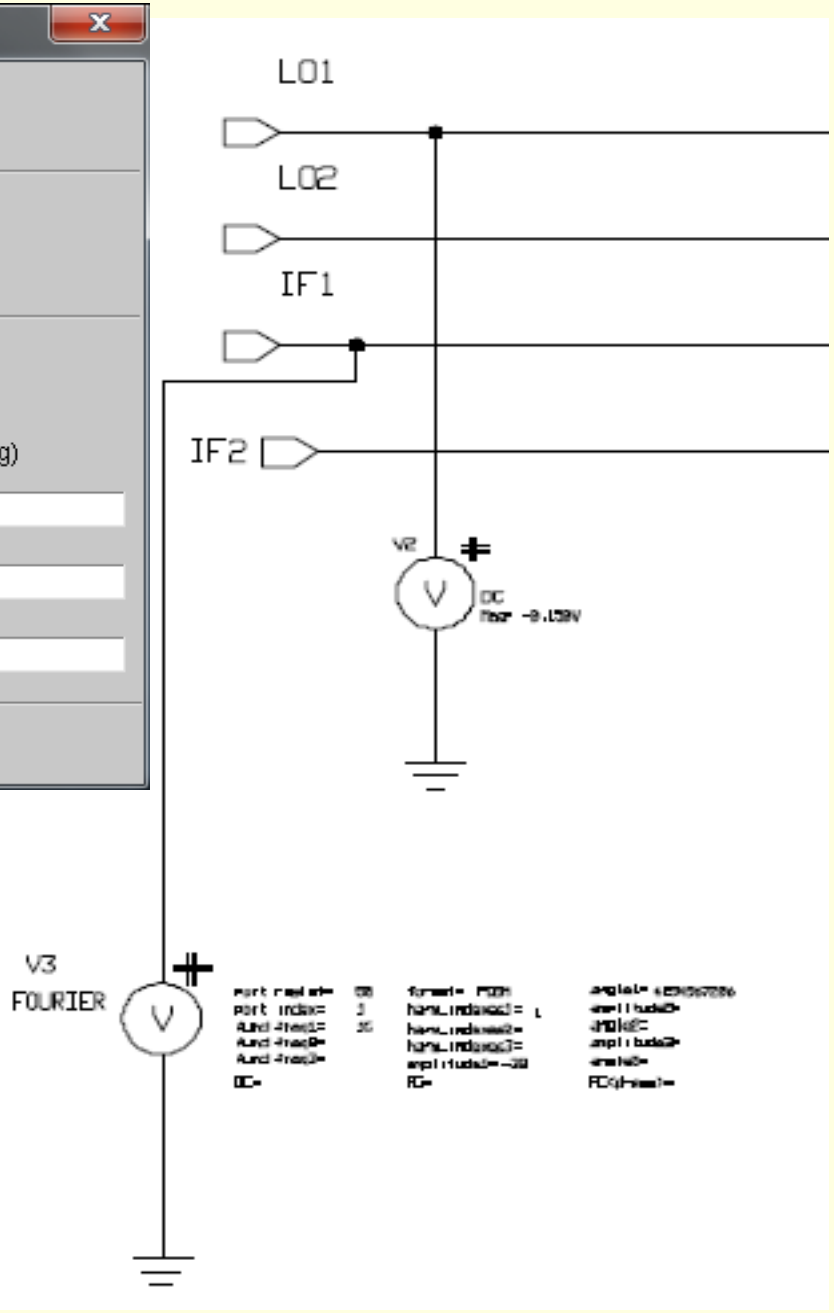
1.



2.-„Q“- okno, definujúce parametre zdroja

Zdroje- Vloženie zdrojov





Overenie správnej funkčnosti návrhu

Check- horná lišta

Check list:

Warnings

Errors -> nutné odstrániť

File Edit View Window Setup Help

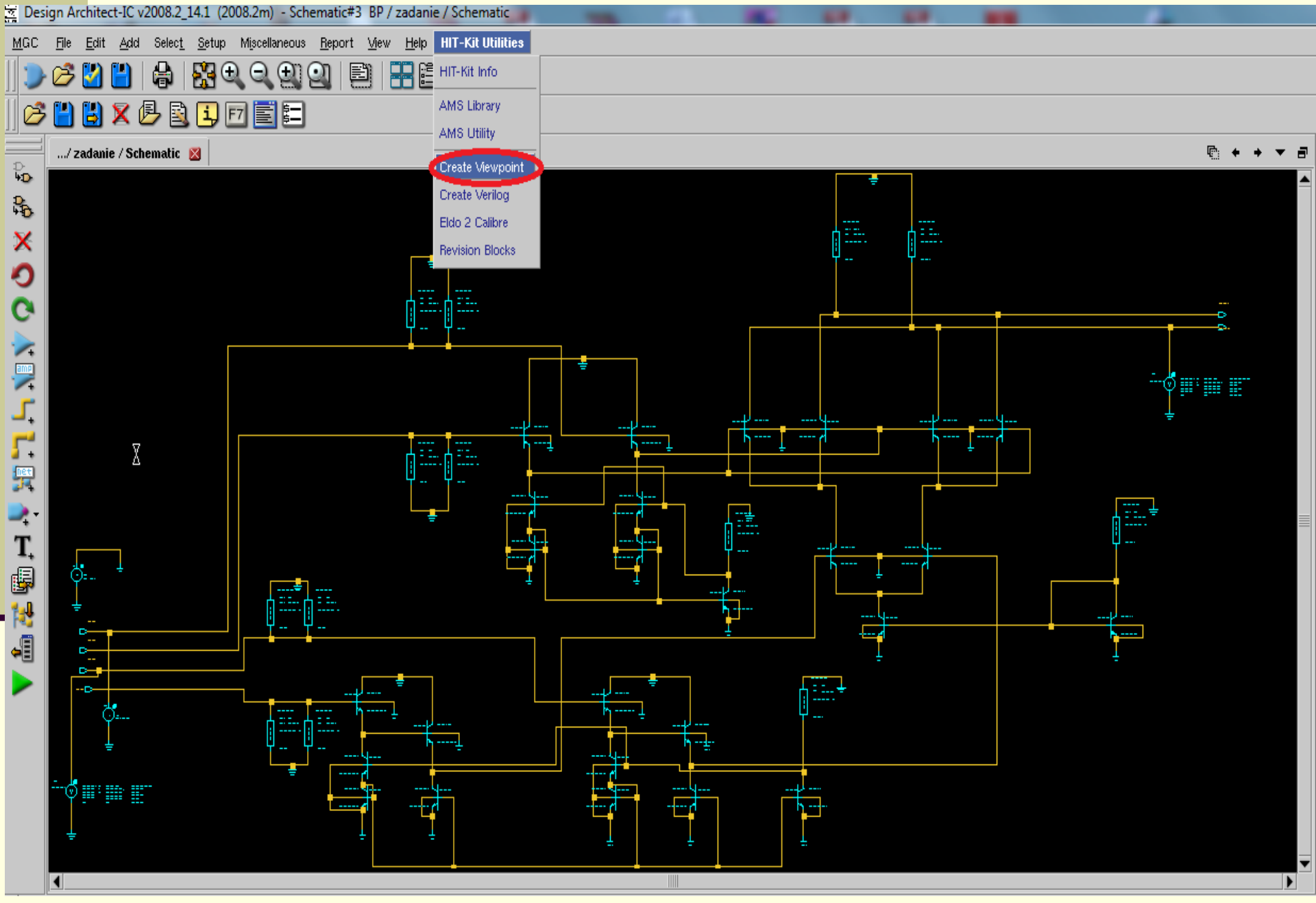
...P / zadanie / Schematic | ...ck#1 zadanie:Report

```
Check Schematic  "zadanie/schematic/sheet1"
Check Sheet "zadanie/schematic/sheet1"
Check SymbolPins --------   0 errors   0 warnings  (MGC-required)
Check Overlap -----------   0 errors   0 warnings
Check NotDots -----------   0 errors   0 warnings
Check Closedots ---------   0 errors   0 warnings
Check Dangle ------------   0 errors   0 warnings
Check UserRule ----------   0 errors   0 warnings
Check Function Blocks ---   0 errors   0 warnings
Check Instance ----------   0 errors               (MGC-required)
Check Special -----------   0 errors   0 warnings  (MGC-required)
Check Net ---------------   0 errors  40 warnings  (MGC-required)
  Warning:  Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
  Warning:  Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
  Warning:  Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
  Warning:  Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
  Warning:  Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
  Warning:  Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
  Warning:  Named net "L01" (N$221) is shorted to Global "ground" at I$100
  Warning:  Named net "vsub" (N$49) is shorted to Global "VEE" at I$25
  Warning:  Named net "vsub" (N$208) is shorted to Global "VEE" at I$31
  Warning:  Named net "vsub" (N$190) is shorted to Global "VEE" at I$79
  Warning:  Named net "vsub" (N$174) is shorted to Global "VEE" at I$73
  Warning:  Named net "vsub" (N$133) is shorted to Global "VEE" at I$60
  Warning:  Named net "vsub" (N$240) is shorted to Global "VEE" at I$87
  Warning:  Named net "vsub" (N$247) is shorted to Global "VEE" at I$28
  Warning:  Named net "vsub" (N$182) is shorted to Global "VEE" at I$76
  Warning:  Named net "vsub" (N$155) is shorted to Global "VEE" at I$77
  Warning:  Named net "vsub" (N$129) is shorted to Global "VEE" at I$59
  Warning:  Named net "vsub" (N$69) is shorted to Global "VEE" at I$34
  Warning:  Named net "vsub" (N$70) is shorted to Global "VEE" at I$35
  Warning:  Named net "vsub" (N$56) is shorted to Global "VEE" at I$29
  Warning:  Named net "vsub" (N$178) is shorted to Global "VEE" at I$68
  Warning:  Named net "vsub" (N$45) is shorted to Global "VEE" at I$23
  Warning:  Named net "vsub" (N$39) is shorted to Global "VEE" at I$24
  Warning:  Named net "vsub" (N$108) is shorted to Global "VEE" at I$49
  Warning:  Named net "vsub" (N$117) is shorted to Global "VEE" at I$50
  Warning:  Named net "vsub" (N$121) is shorted to Global "VEE" at I$52
```

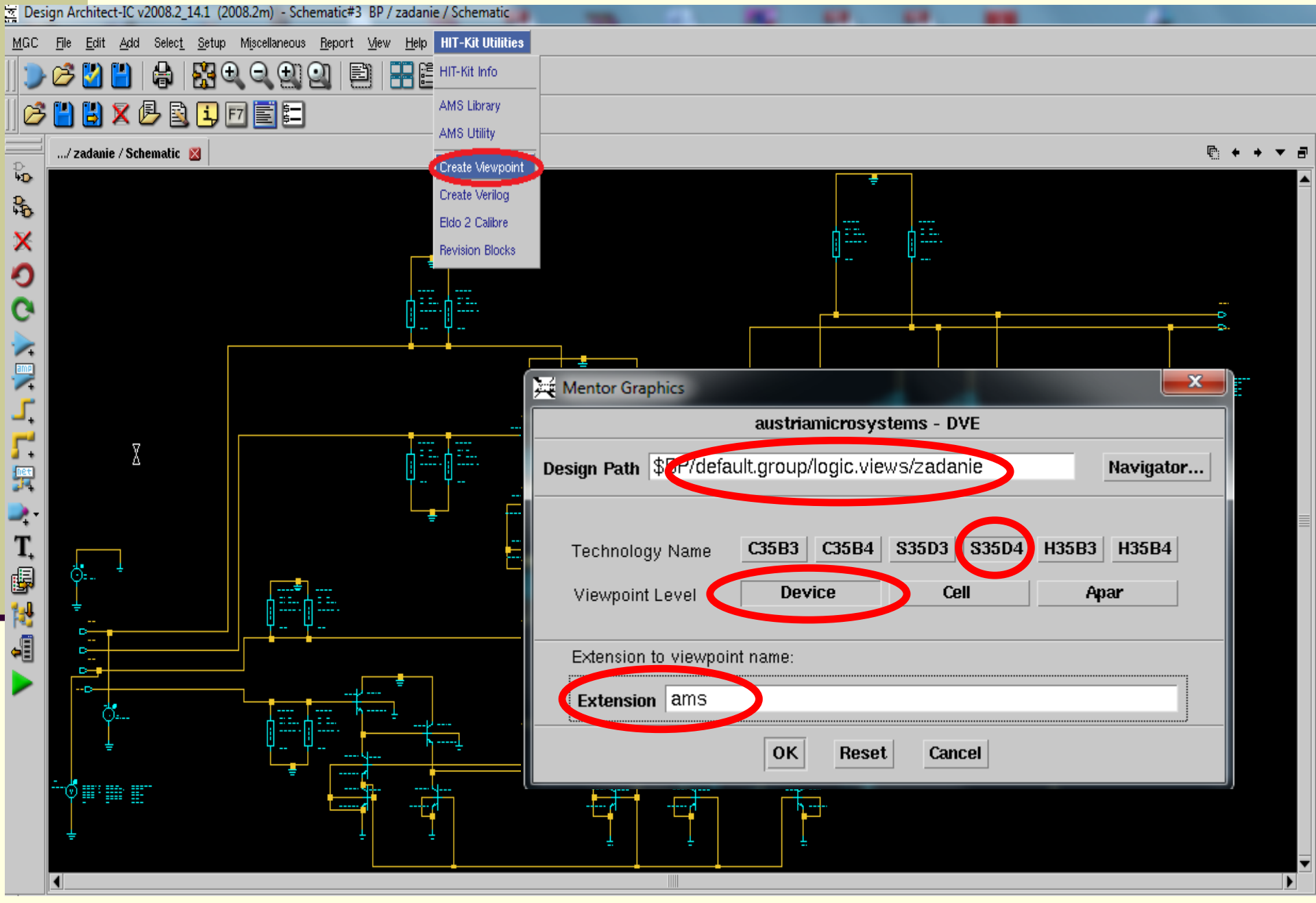
session

Open
Schematic
Symbol
Setup
Display
Property Display
Report
Check Schematic
Check Symbol
Print
Session

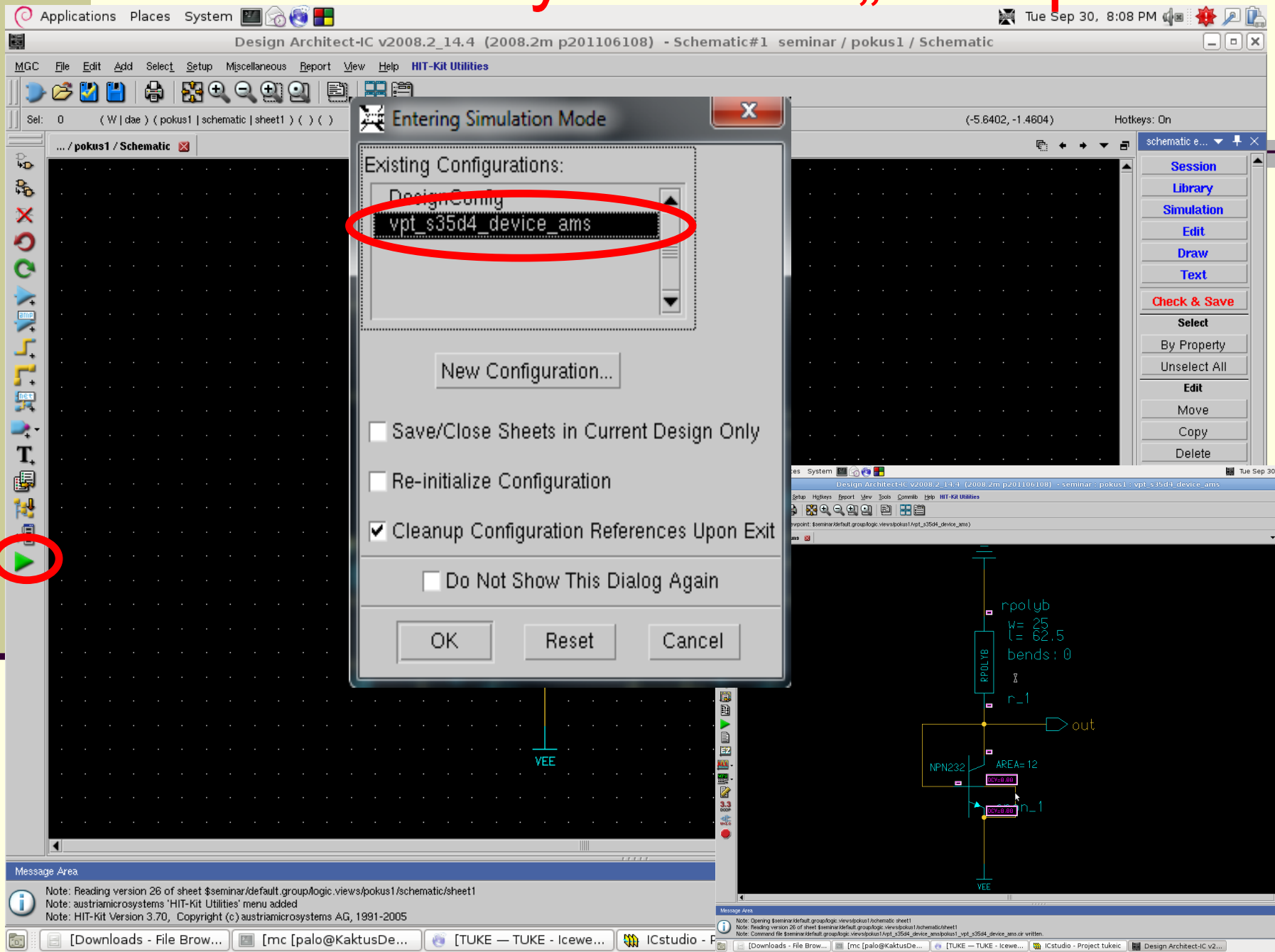
Simulácia- vytvorenie „Viewpoint“



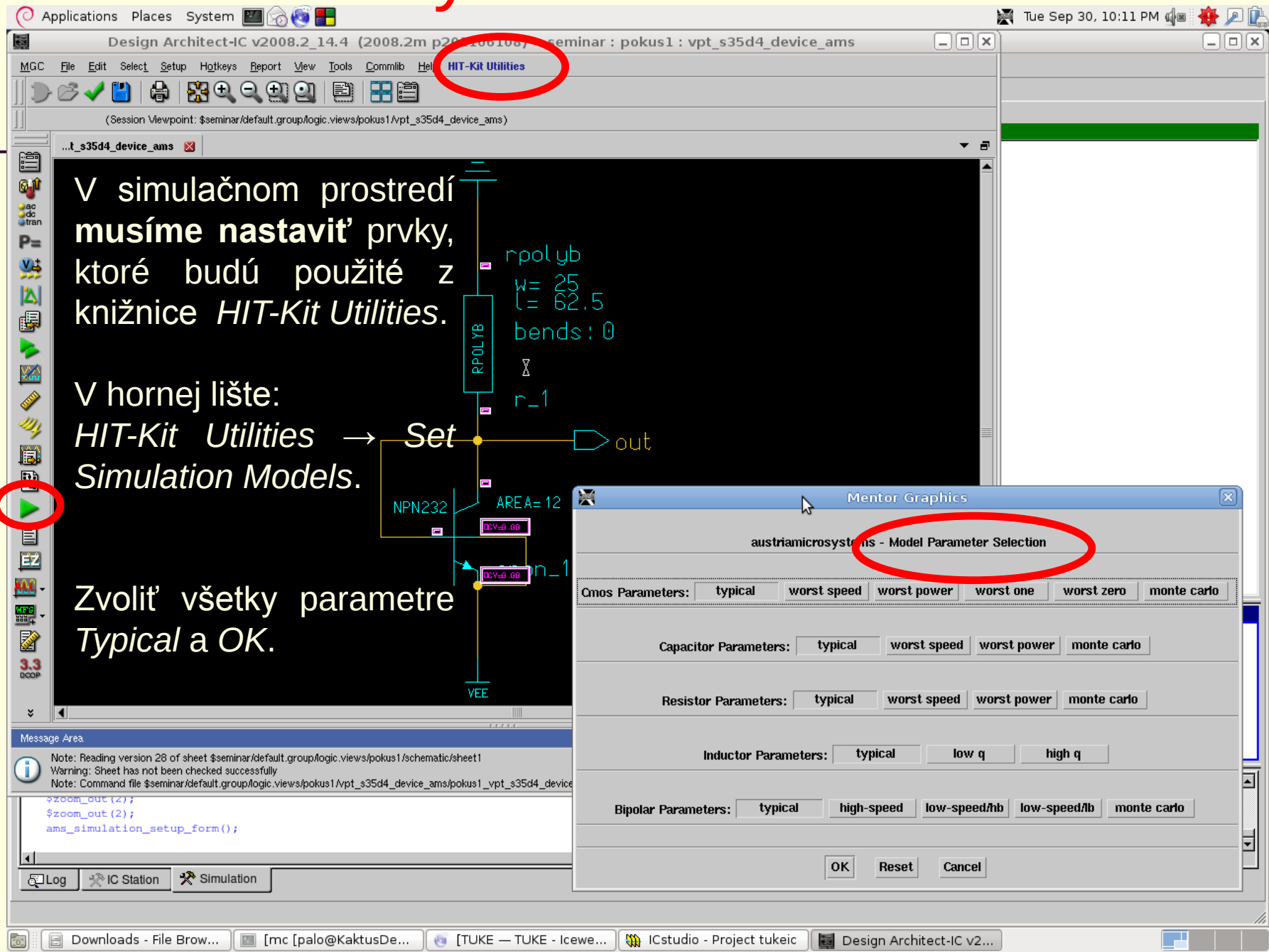
Simulácia- vytvorenie „Viewpoint“



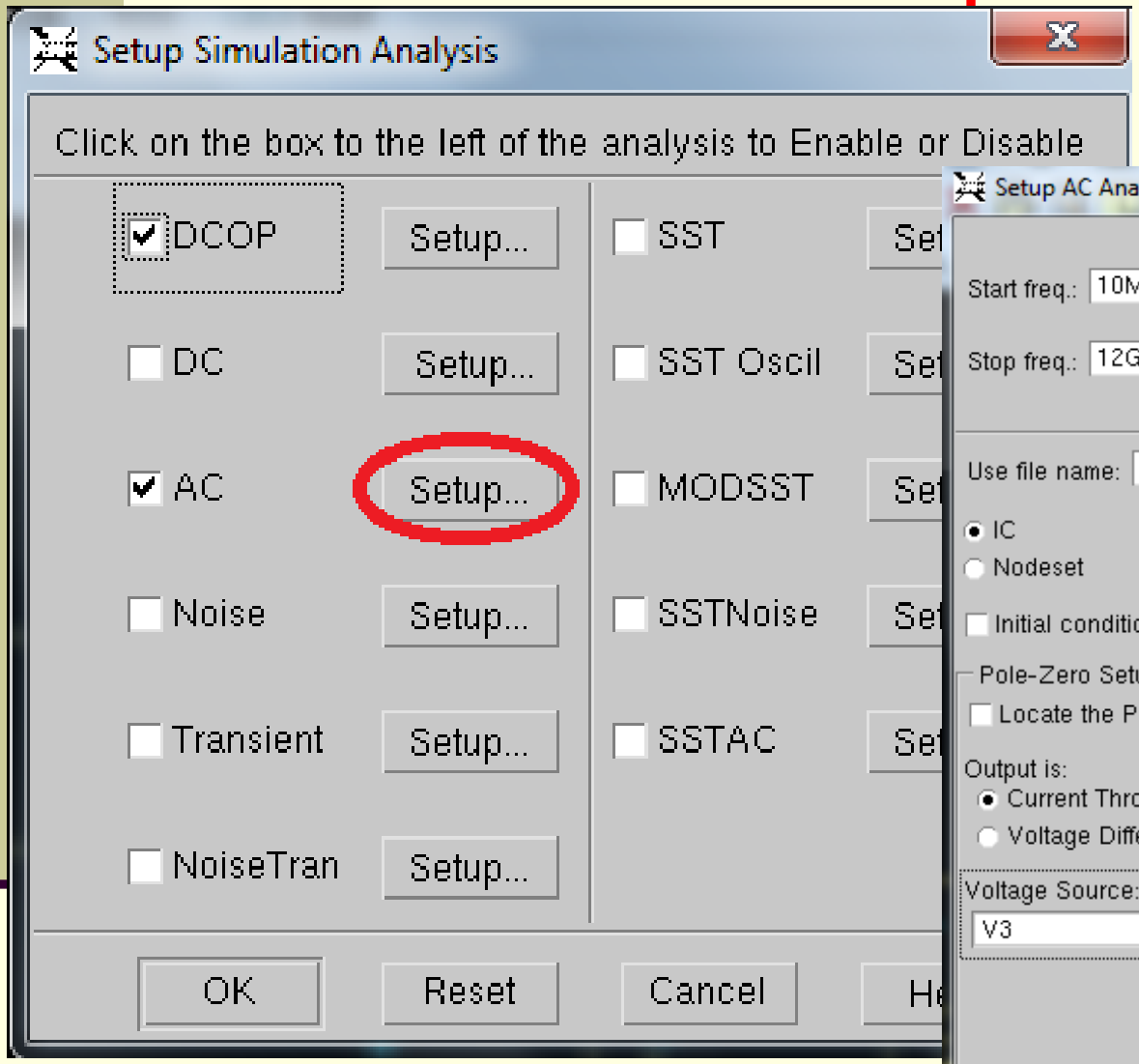
Simulácia- vytvorenie „Viewpoint“

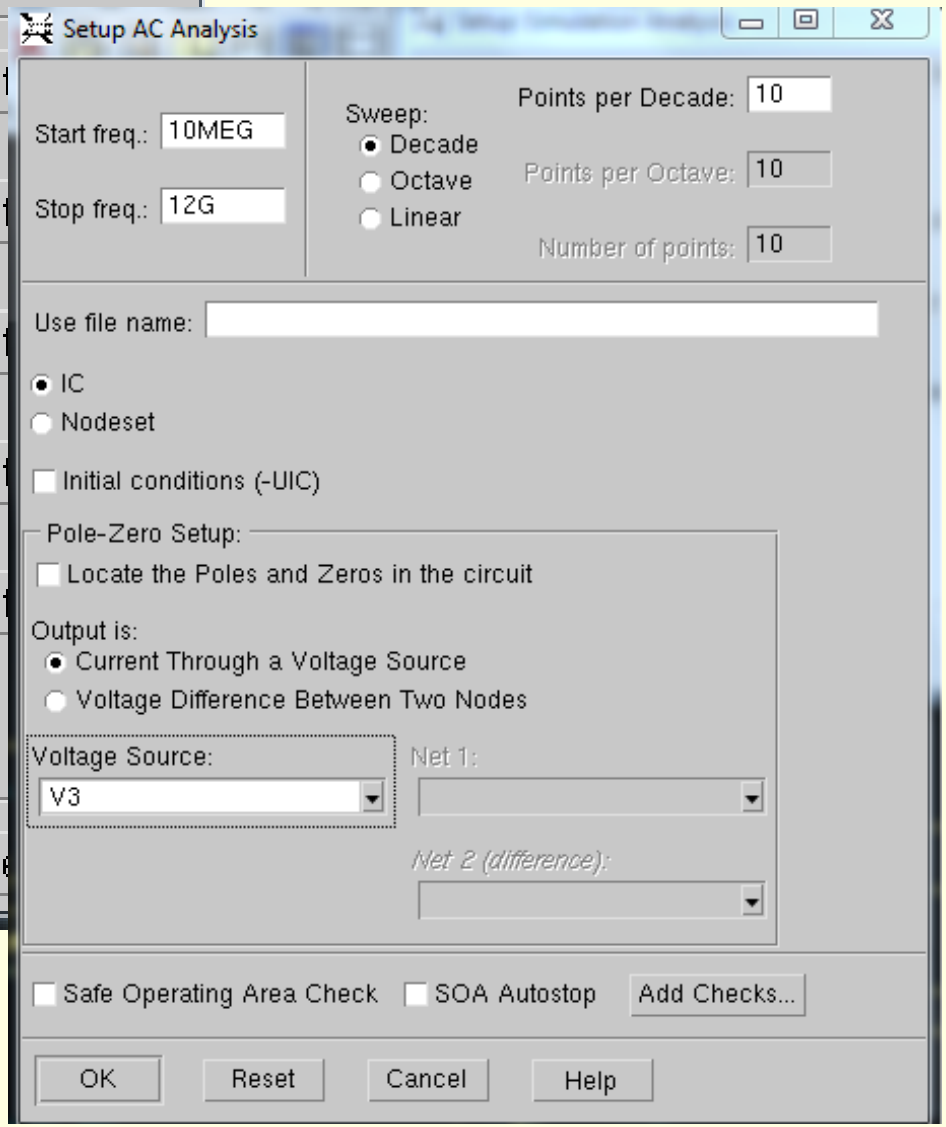


Simulácia- výber modelov



Simulácia ▶ Setup Analysis

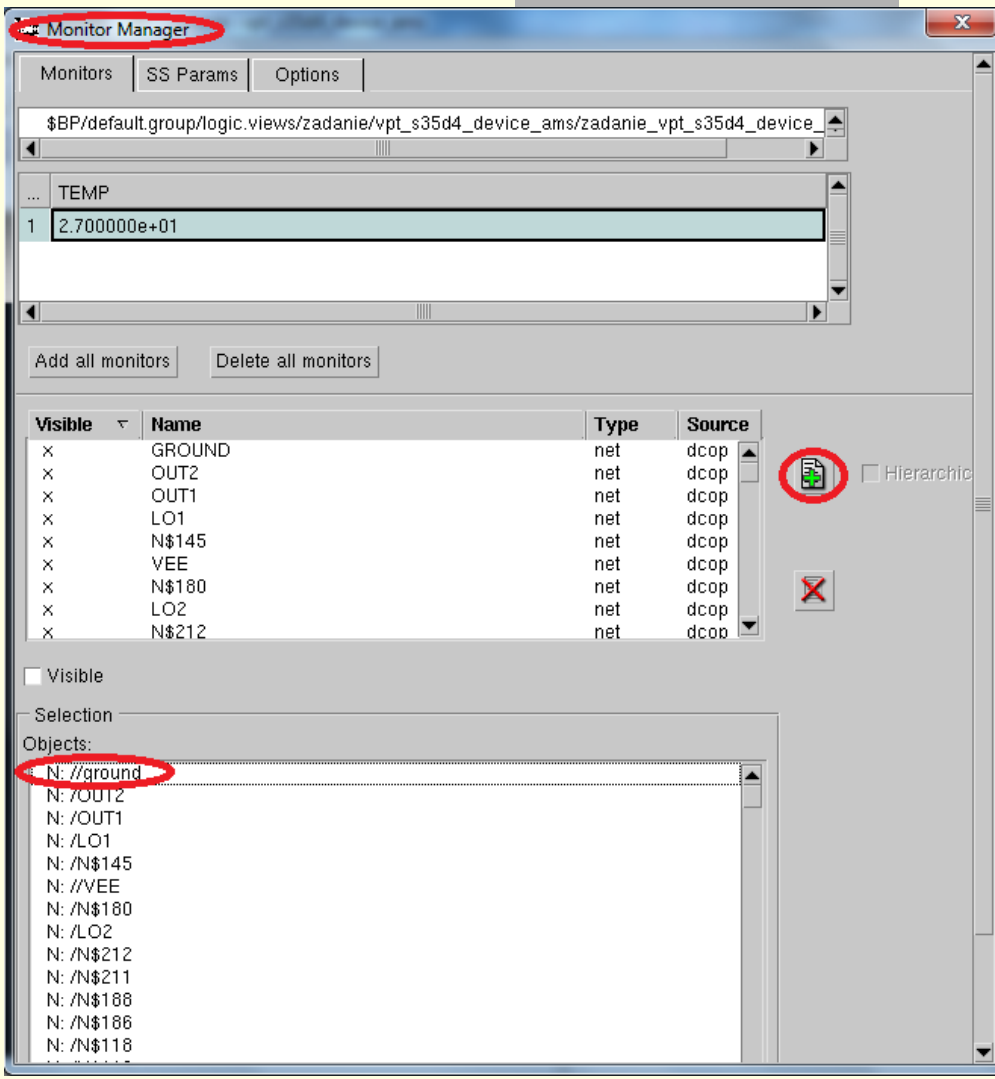




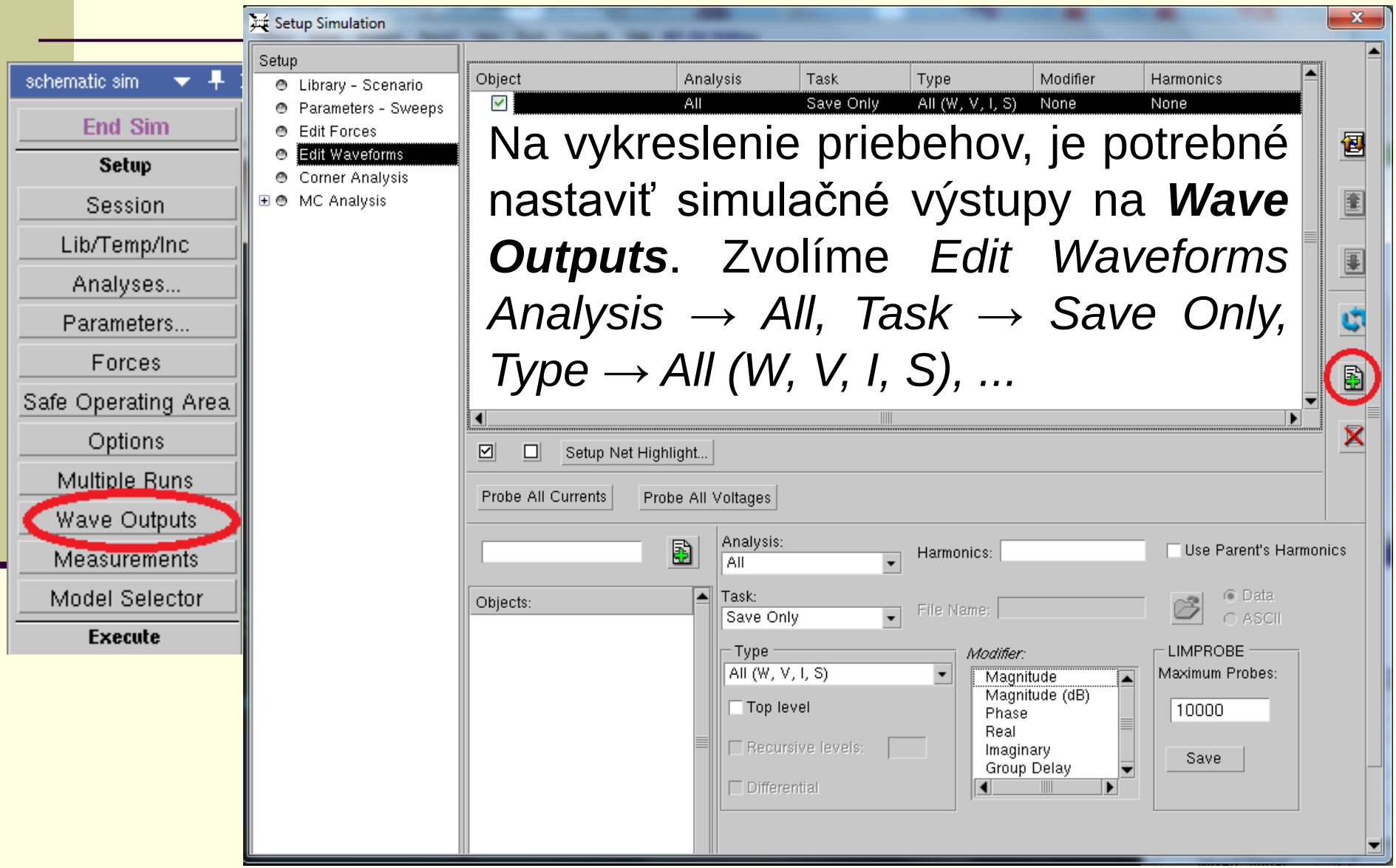
Simulácia -> nastavenie vykreslenia napätí a prúdov

Označíme celú schému obvodu a klikneme na ***DCOP/TRAN.***

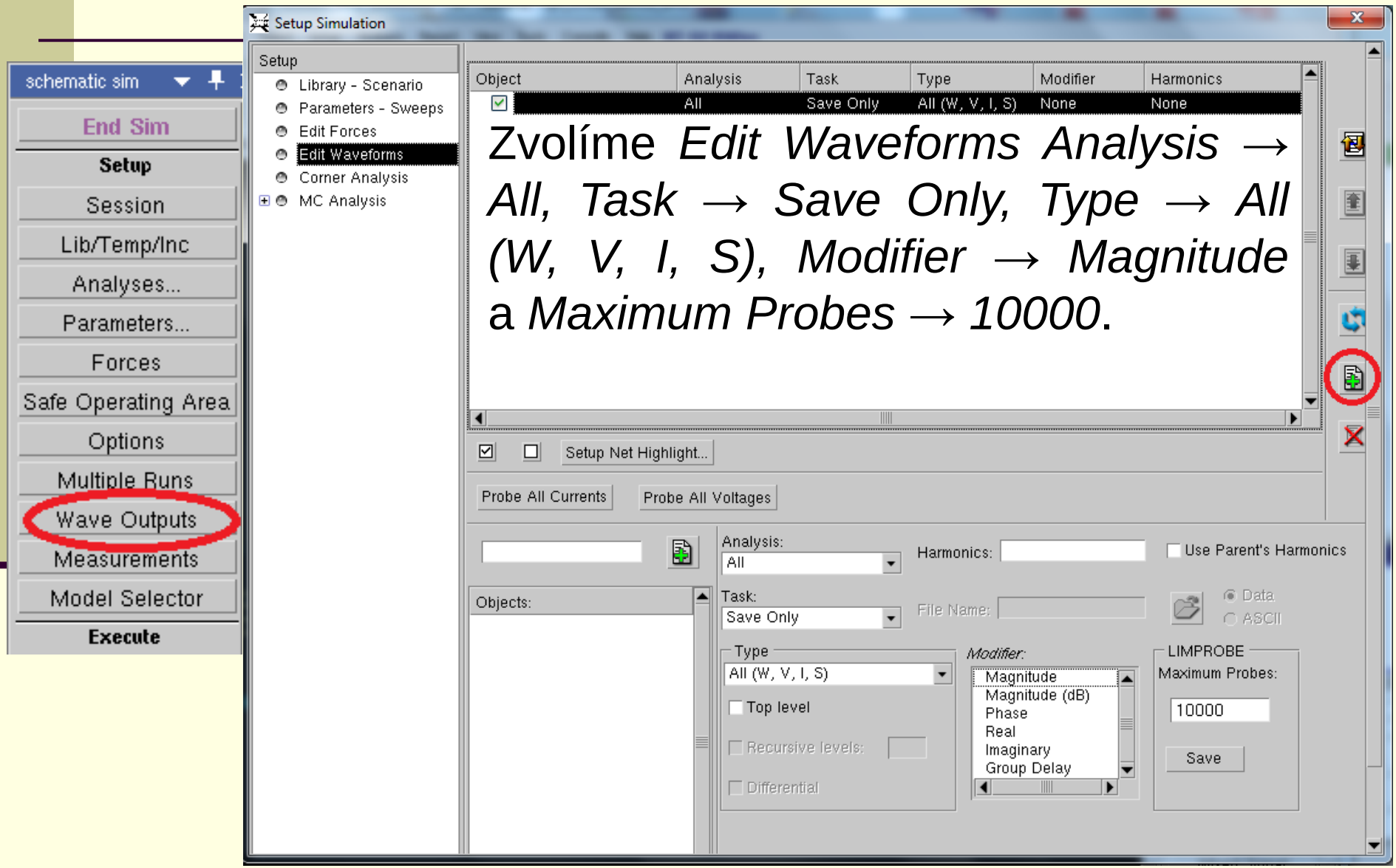
V obvode sa objavia hodnoty napätí a prúdov.



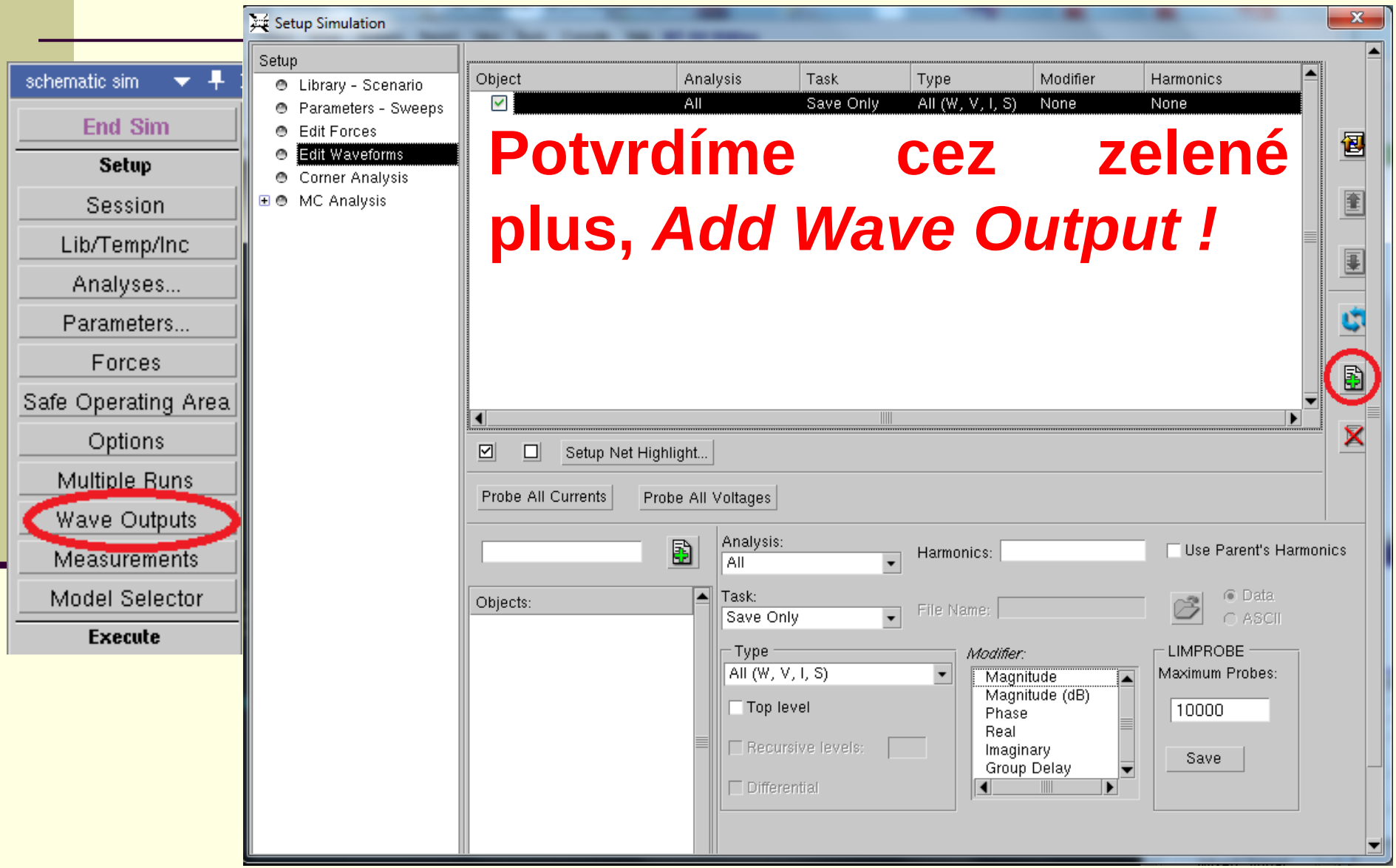
Simulácia -> Zobrazenie výstupov



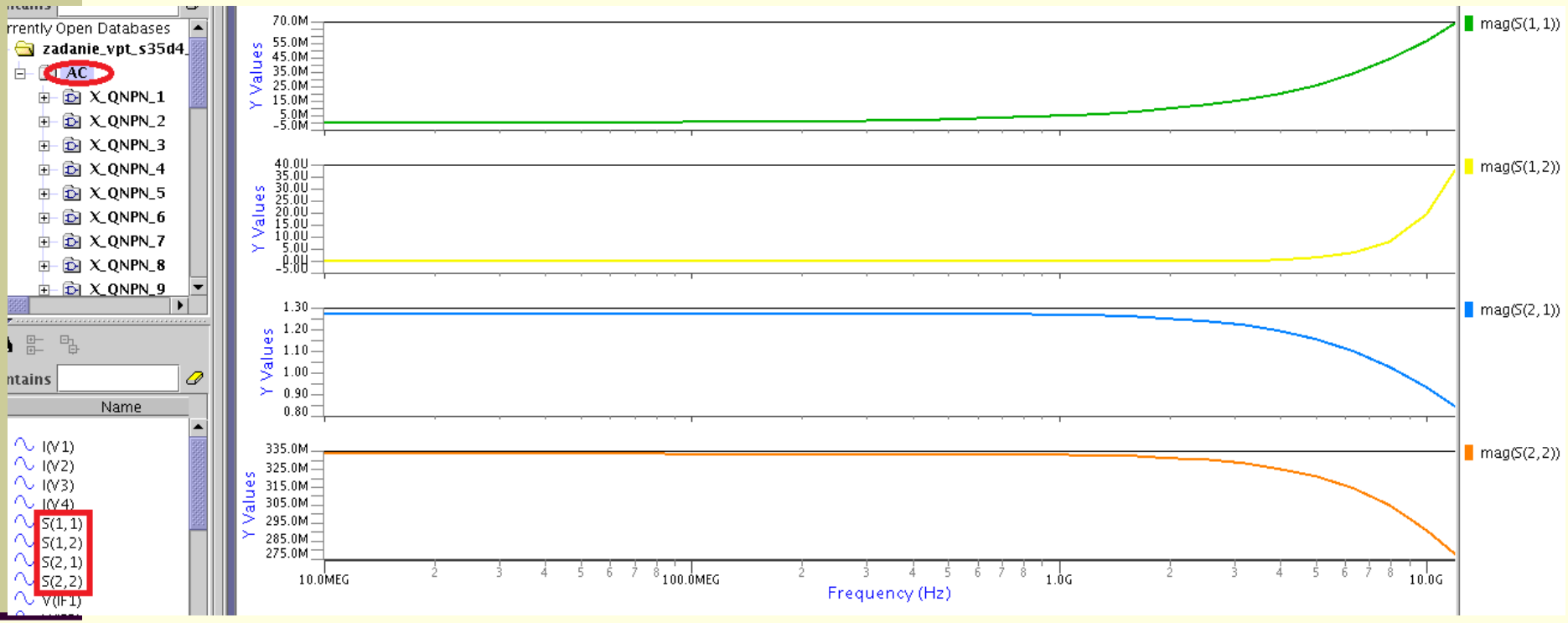
Simulácia -> Zobrazenie výstupov



Simulácia -> Zobrazenie výstupov



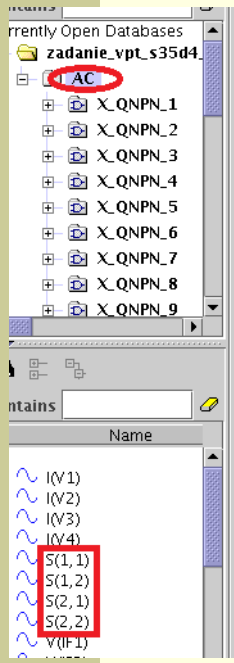
Simulácia -> Vykreslenie simulácií

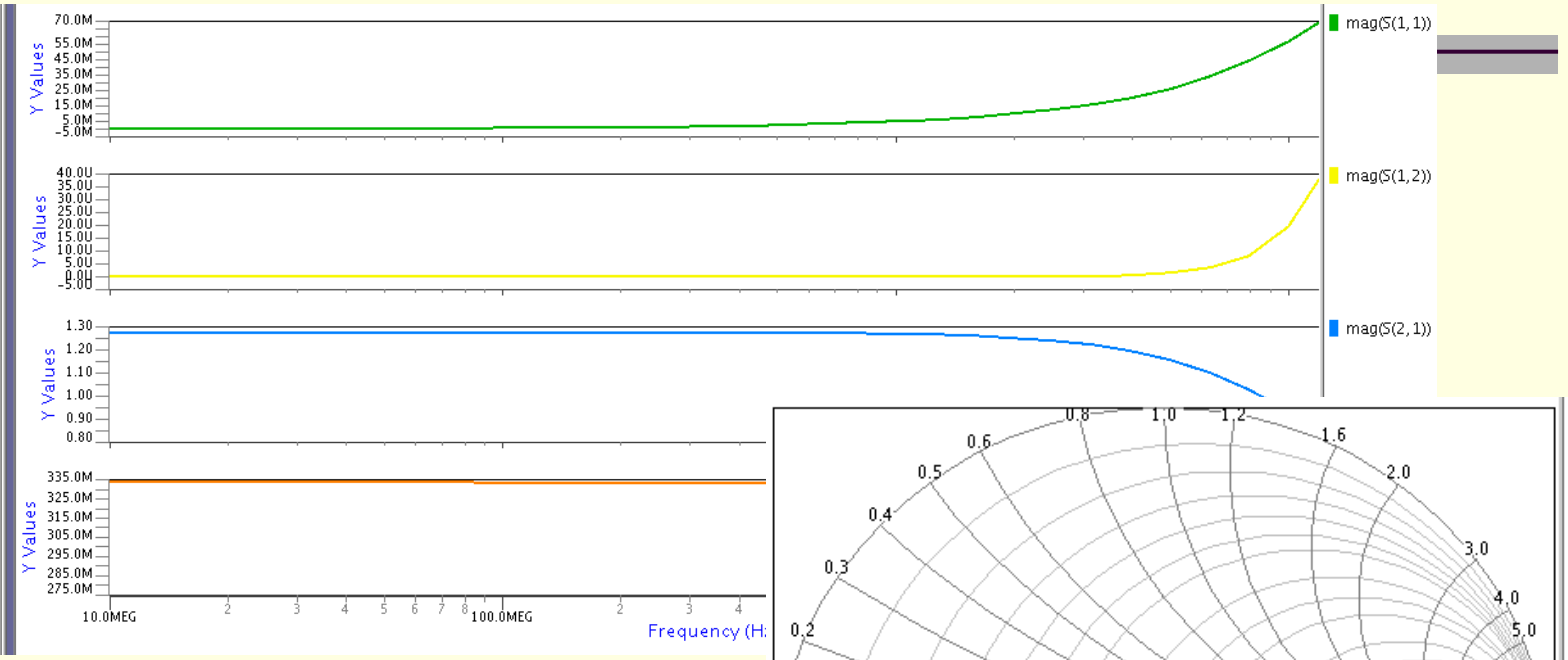


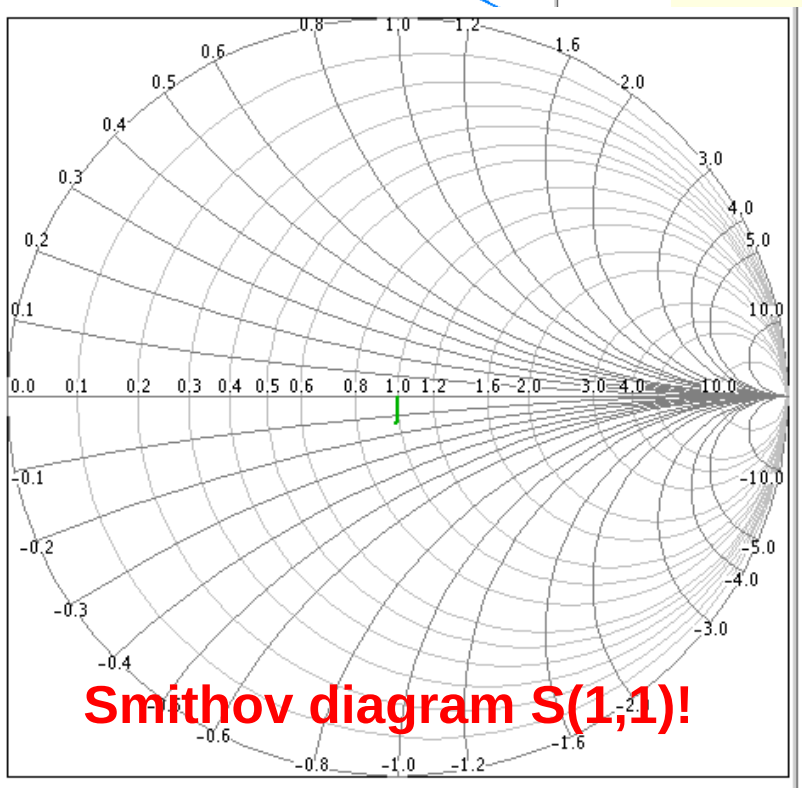
Vľavo dole *View Outputs*, ktorý nám umožňuje vykreslenie jednotlivých priebehov v rôznych jednotkách, alebo diagramoch, ako napríklad v Smithov-om diagrame.

S parameter- ponuka *Plot as → db, magnitude, real, smith_chart*

Simulácia -> Vykreslenie simulácií







Smithov diagram S(1,1)!

End Sim Mode:

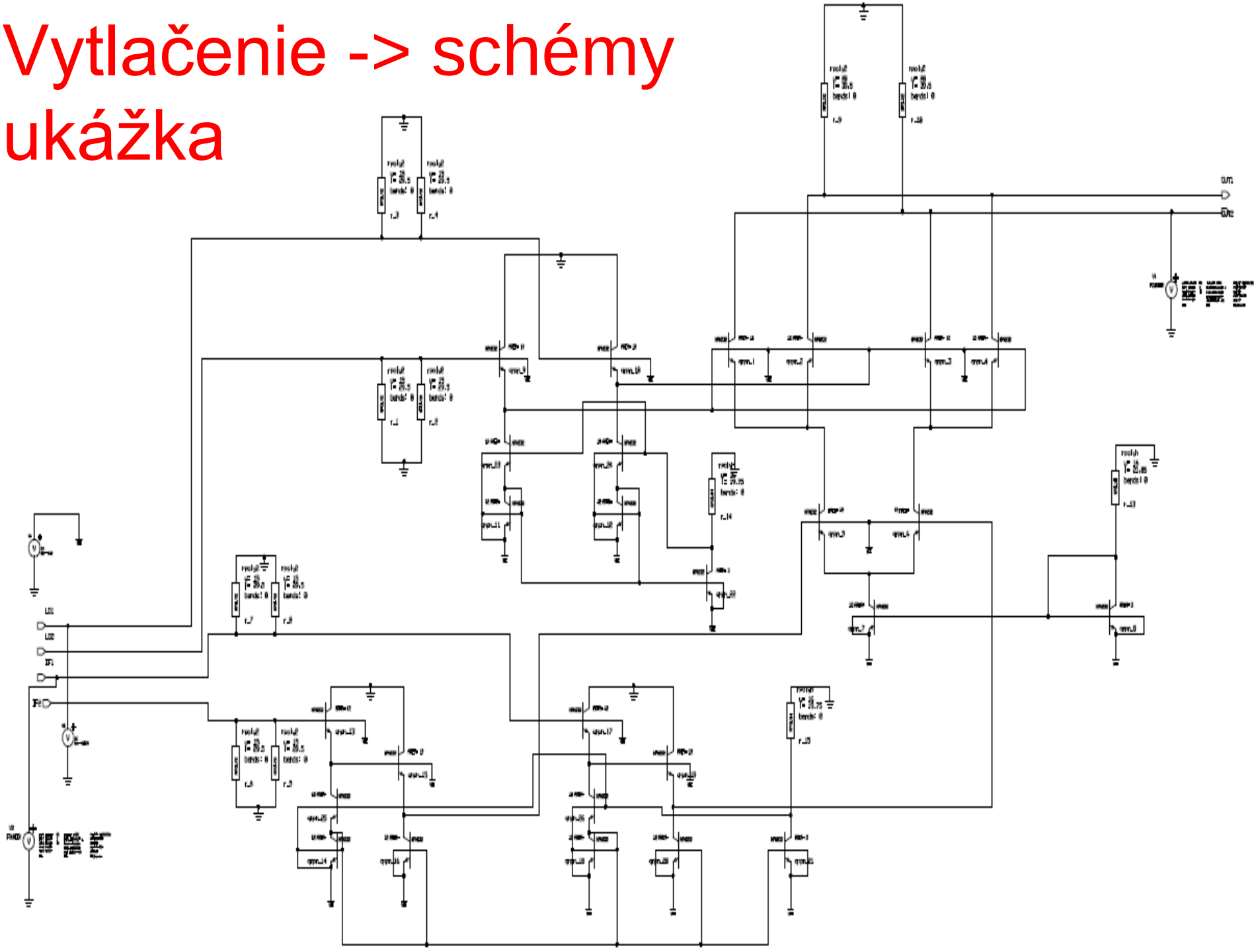
Zo **simulačného** prostredia do **návrhového**

Vytlačenie -> schémy

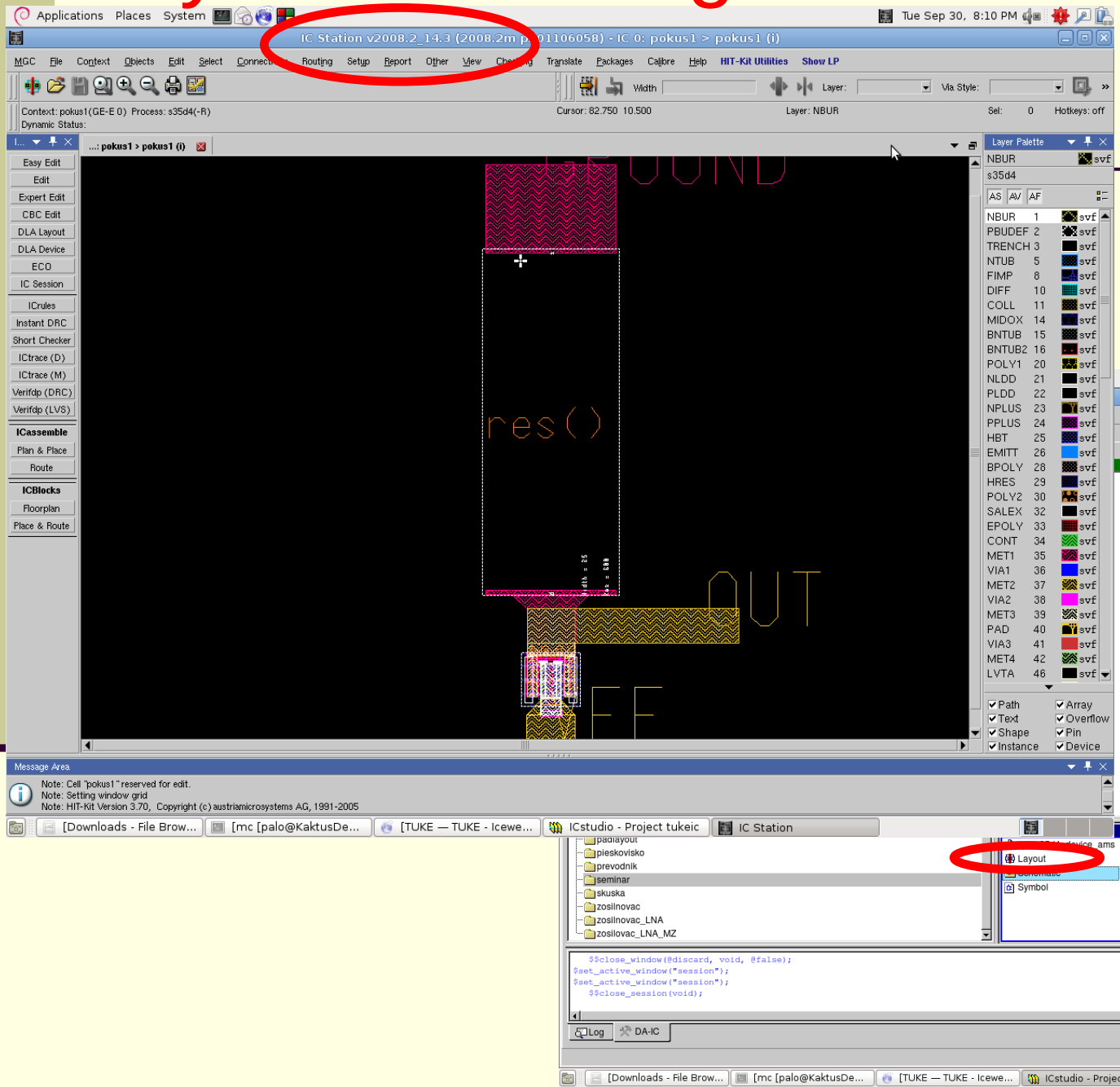
Hlavna lišta *Print*
Print Name → *PDF*
Veľkosť strany → požadovaný formát
Necháme R*otation* → *Best Fit*
Output Format → *Basic PostScript*
Color → *Monochrome* (pre lepšiu čitateľnosť)

Schéma sa uloží v domovskom priečinku

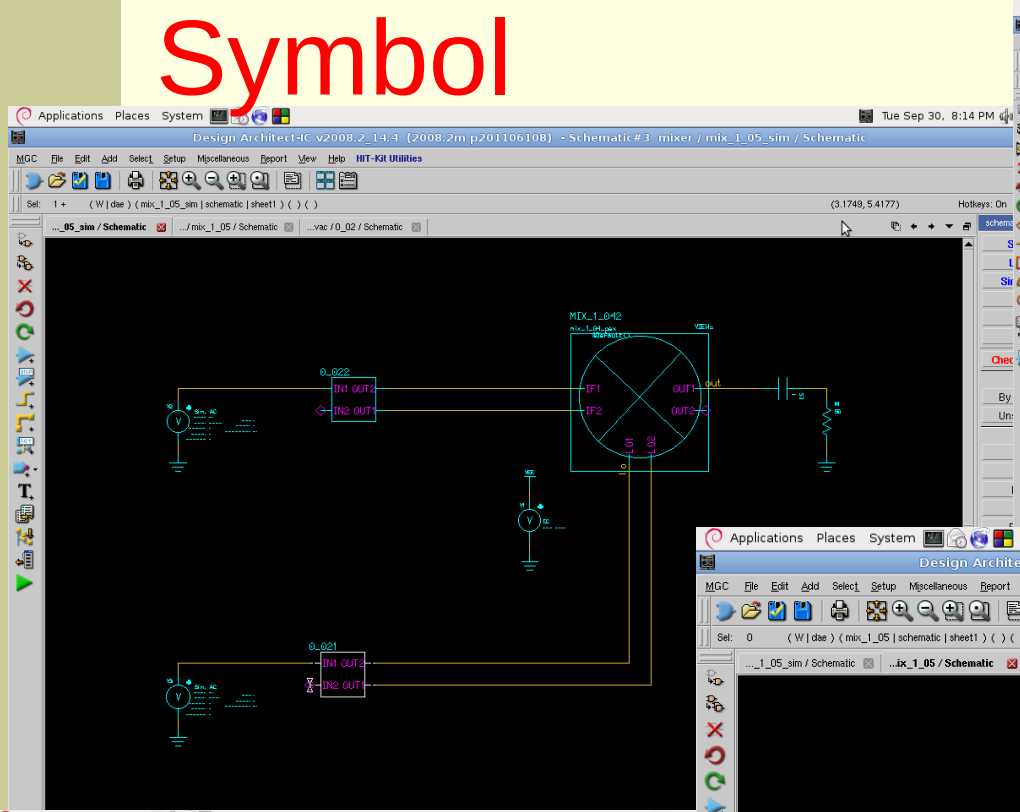
Vytlačenie -> schémy ukážka

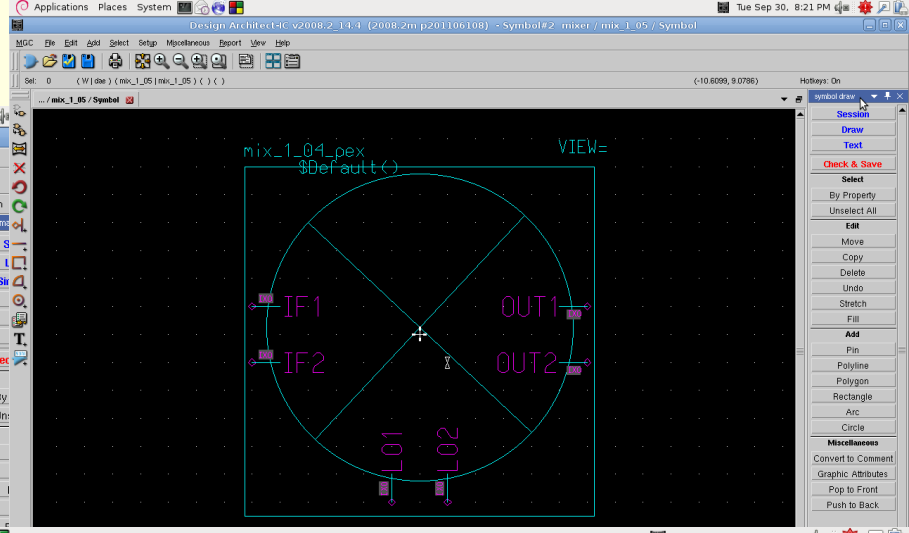


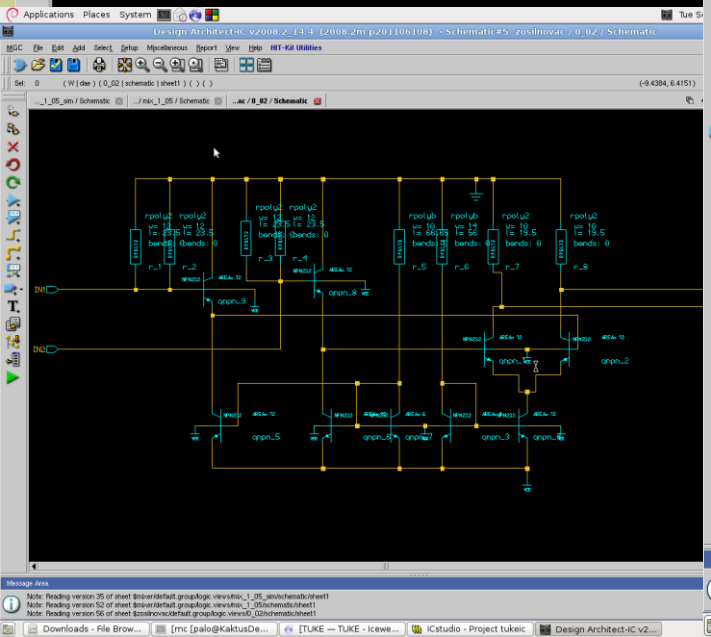
Layout- morfológia masiek

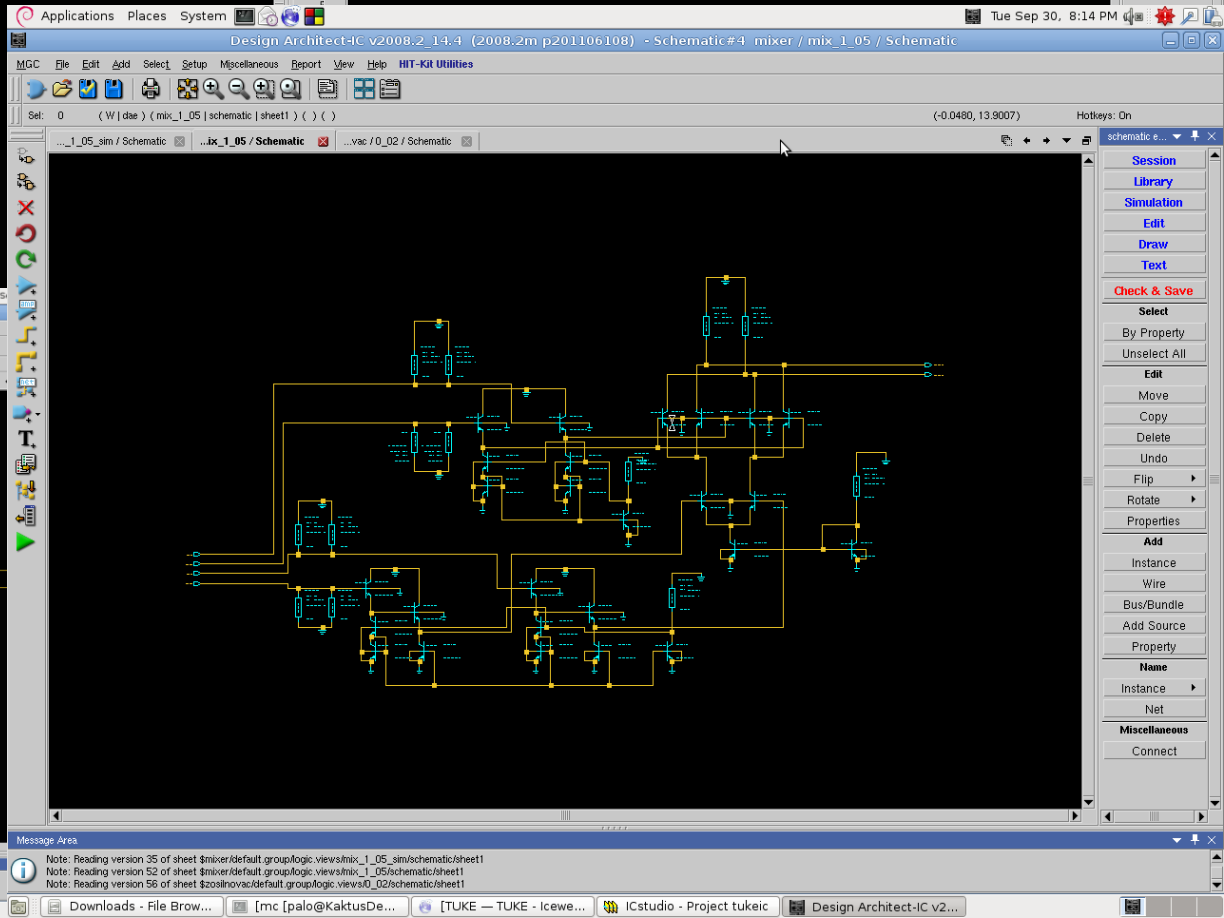


Symbol

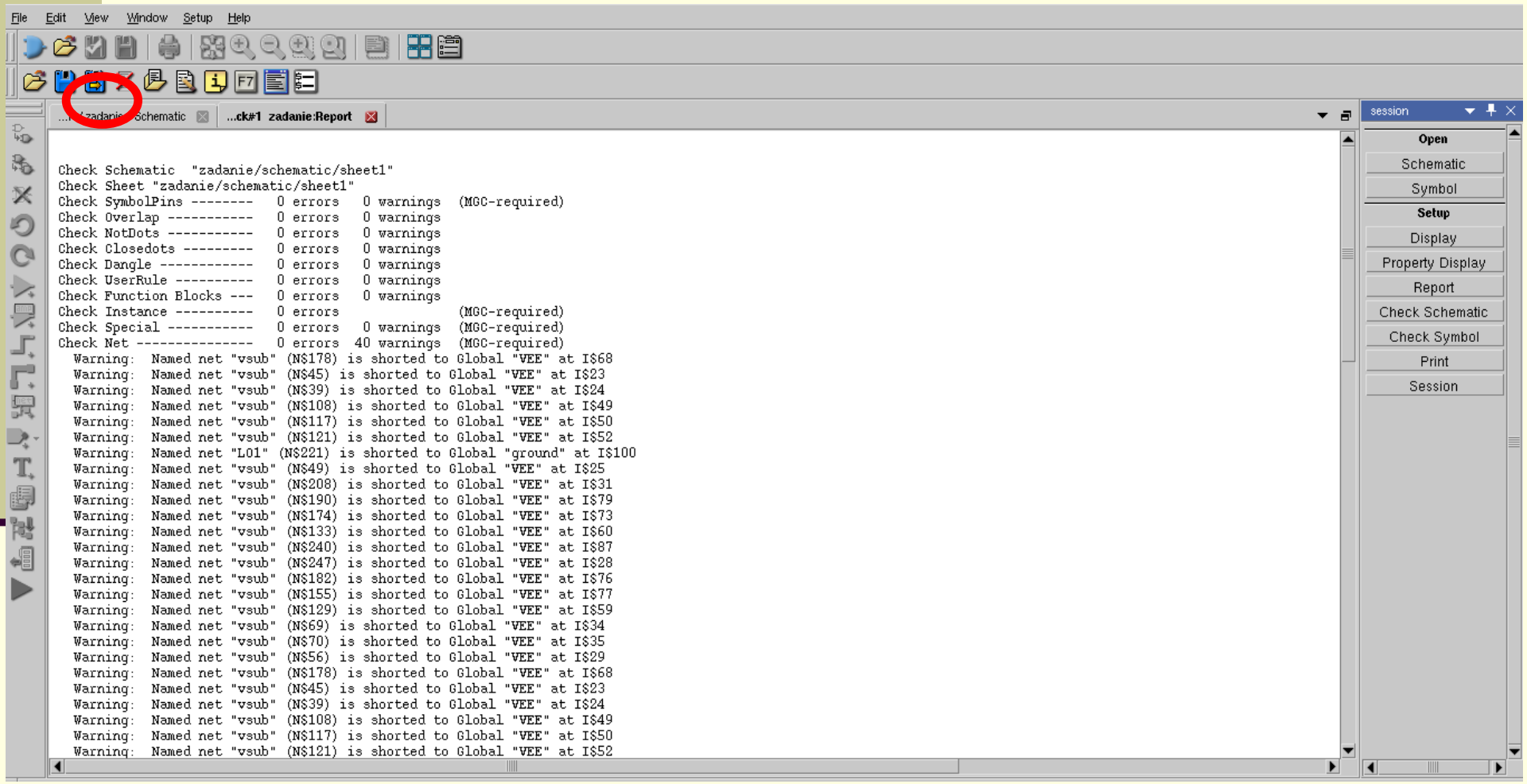

Applications Places System
Tue Sep 30, 8:14 PM
Design Architect-IC v2008.2_14.4 (2008.2m p201106108) - Schematic#3 mixer / mix_1_05_sim / Schematic
MGC File Edit Add Select Setup Miscellaneous Report View Help HIT-Kit Utilities
MIX_1_042
0_022
0_021
IN1 OUT2
IN2 OUT1
IF1
IF2
OUT1
OUT2


Applications Places System
Tue Sep 30, 8:21 PM
Design Architect-IC v2008.2_14.4 (2008.2m p201106108) - Symbol#2 mixer / mix_1_05 / Symbol
mix_1_04_pex
$Default()
VIEW=
IF1
IF2
OUT1
OUT2
LO1
LO2


Applications Places System
Design Architect-IC v2008.2_14.4 (2008.2m p201106108) - Schematic#5 zosilnovac / 0_02 / Schematic
IN1
IN2


Applications Places System
Tue Sep 30, 8:14 PM
Design Architect-IC v2008.2_14.4 (2008.2m p201106108) - Schematic#4 mixer / mix_1_05 / Schematic
MGC File Edit Add Select Setup Miscellaneous Report View Help HIT-Kit Utilities
Session
Library
Simulation
Edit
Draw
Text
Check & Save
Select
By Property
Unselect All
Move
Copy
Delete
Undo
Flip
Rotate
Properties
Add
Instance
Wire
Bus/Bundle
Add Source
Property
Name
Net
Miscellaneous
Connect
Message Area
Note: Reading version 35 of sheet $mixer/default.group/logic.views/mix_1_05_sim/schematic/sheet1
Note: Reading version 52 of sheet $mixer/default.group/logic.views/mix_1_05/schematic/sheet1
Note: Reading version 56 of sheet $zosilnovac/default.group/logic.views/0_02/schematic/sheet1
Downloads - File Brow...
[mc [palo@KaktusDe...
[TUKE — TUKE - Icewe...
ICstudio - Project tukeic
Design Architect-IC v2...

Overenie správnej funkčnosti návrhu



Europractice IC mission

- **Prototyping**
- Multi Project Wafer Runs (MPWs)
- Design Kits
- Prototype testing
- Prototype encapsulations (packaging)
- EDA support

http://www.europractice-ic.com/prototyping.php

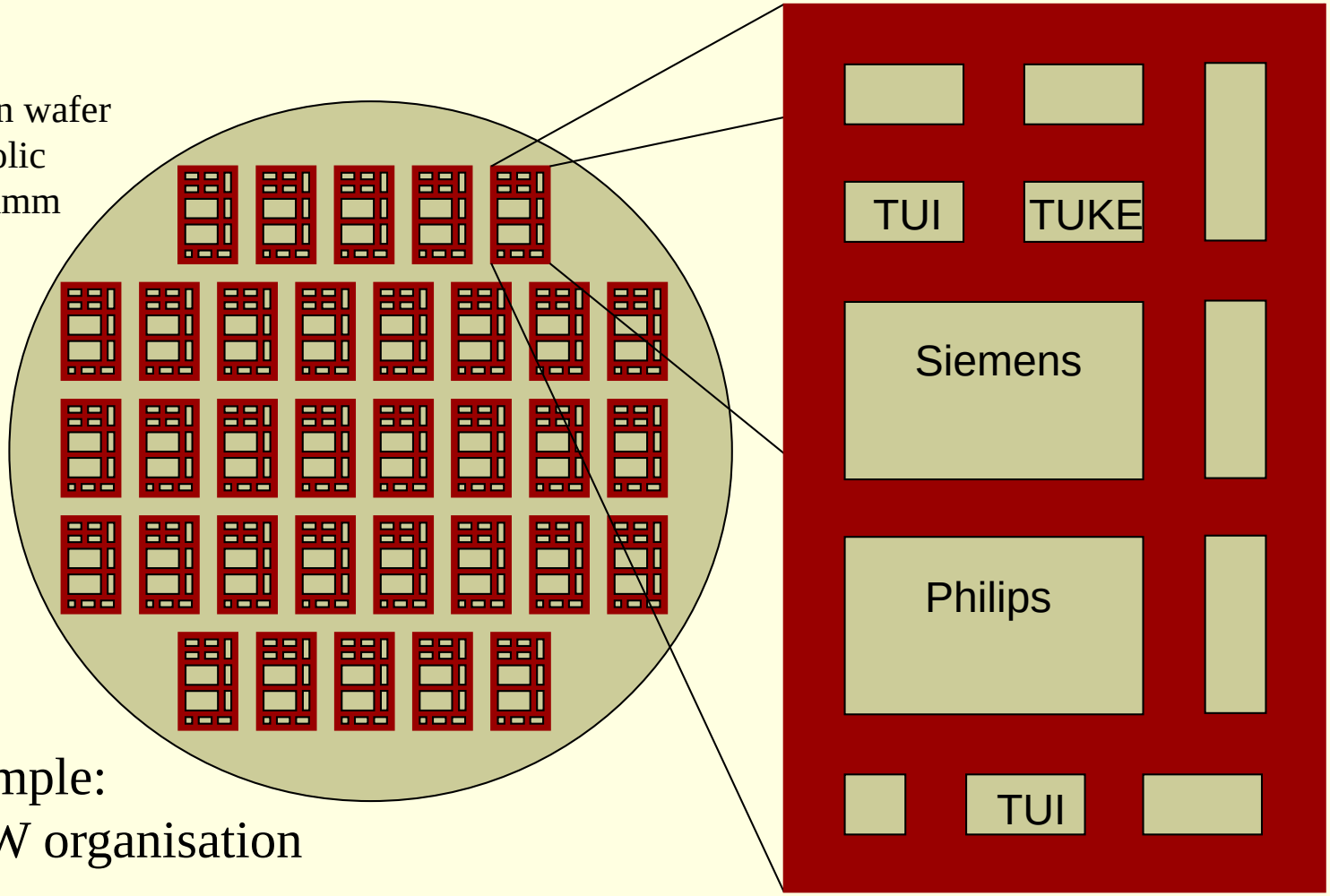
- **Volume Production**
- Low cost after prototype fabrication service
- Packaging and tests
- ASIC qualification
- Technical support

EUROPRACTICE

http://www.europractice-ic.com/volume_production.php

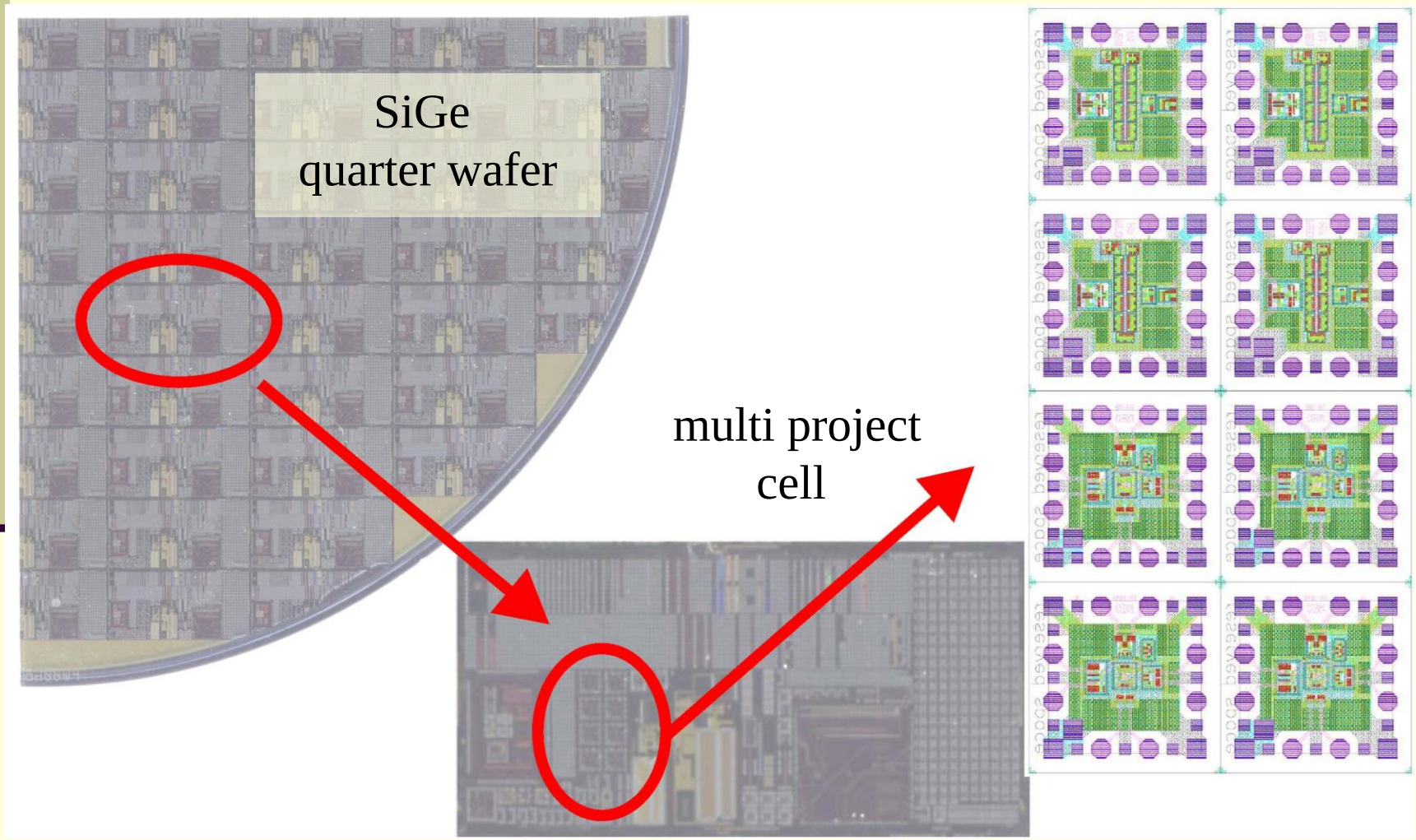
MPW ~ multi-project wafer

Silicon wafer symbolic diagramm

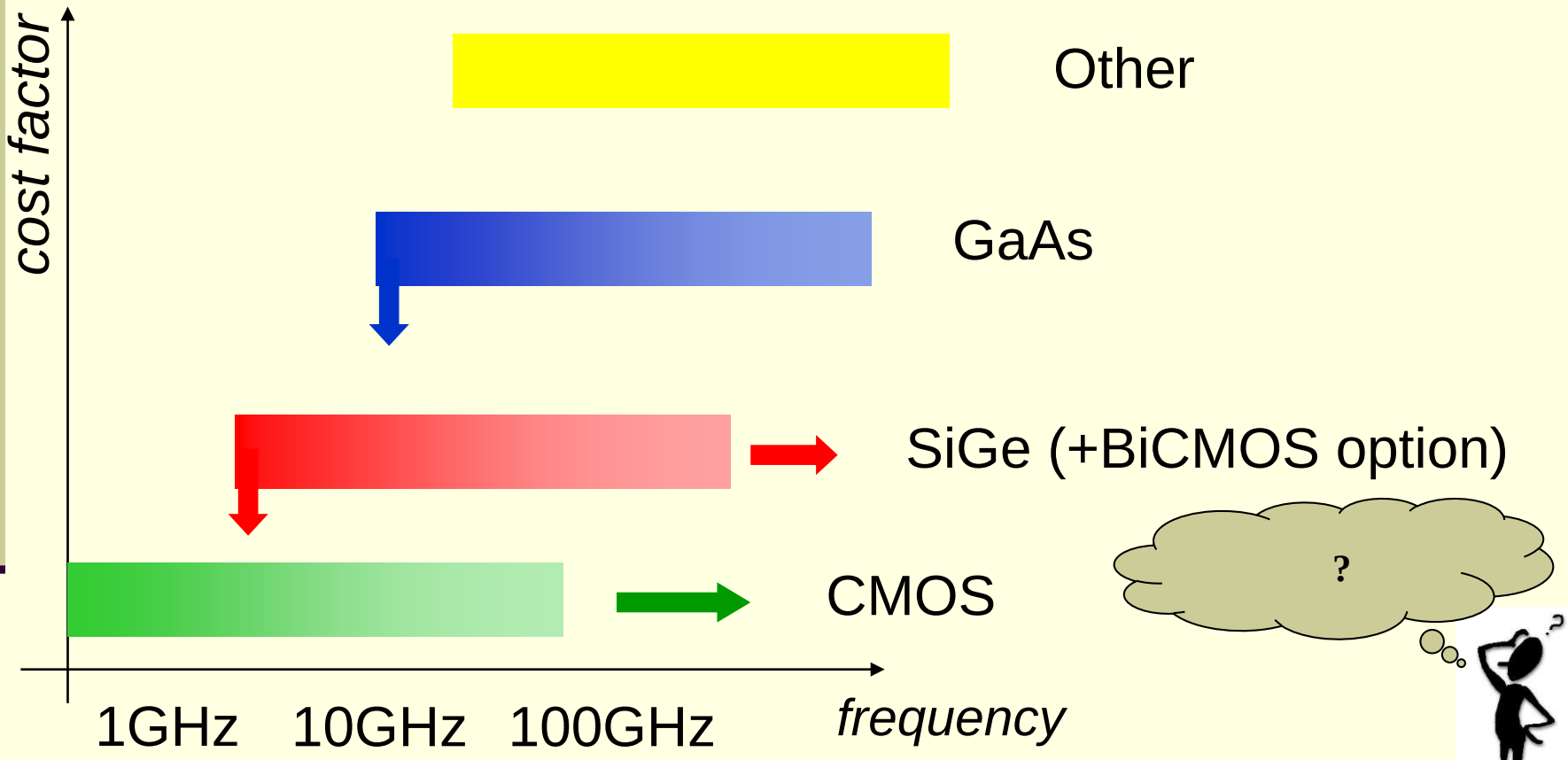


Example:
MPW organisation

MPW ~ prototyping example



IC technology aspects



Other considerations: **SNR** (SiGe), **Linearity** (CMOS), **Modelling** (SiGe) **…**

EU MPW available technologies

austriamicrosystems

CMOS - 0,8μm; 0,35μm; 0,18μm
BiCMOS - 0,35μm

AMI SEMICONDUCTOR

CMOS - 0,7μm; 0,5μm; 0,35μm

ihp

BiCMOS - 0,25μm; 0,13μm
(Ft up to 300GHz)

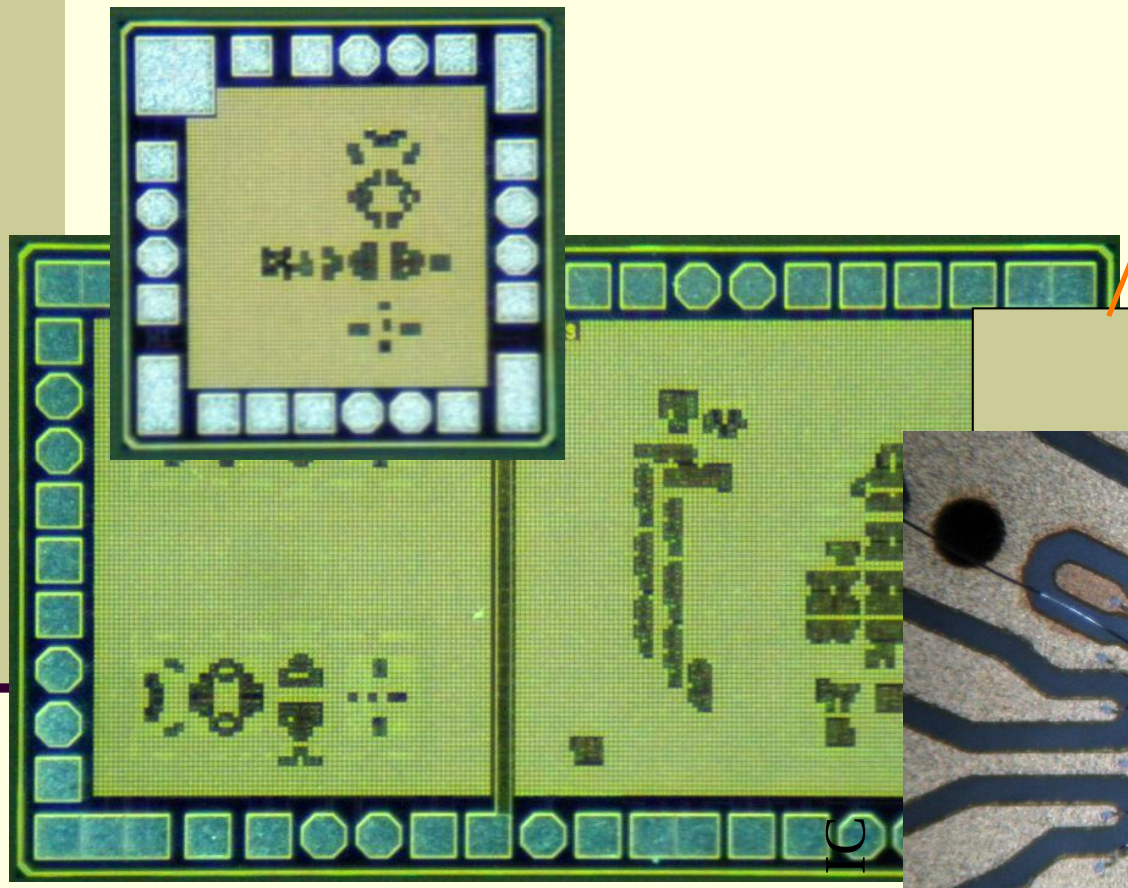
tsmc

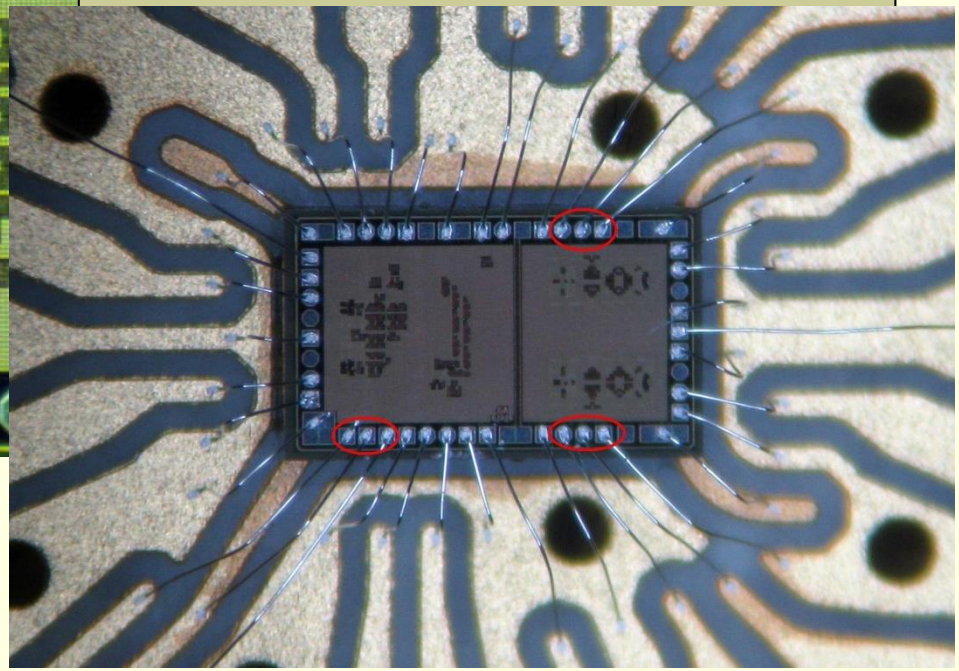
CMOS - 0,25μm; 0,13μm
(… 45nm)

*EUROPRACTICE SUPPORTED processes, selected technologies

Source: EUROPRACTICE

Examples of IC prototypes





bonding

bond wire

IC

IC carrier or package

Bonded IC

Examples of IC prototypes