

1 Introduction

Feature	2101	2103	2105	2115	2111	2171	2173	2181	2183	21msp58
Arithmetic/Logic Unit	•	•	•	•	•	•	•	•	•	•
Multiply/Accumulator	•	•	•	•	•	•	•	•	•	•
Shifter	•	•	•	•	•	•	•	•	•	•
Data Address Generators	•	•	•	•	•	•	•	•	•	•
Program Sequencer	•	•	•	•	•	•	•	•	•	•
Data Memory RAM	1K	1K	512	512	1K	2K	2K	16K	16K	2K
Program Memory RAM	2K	2K	1K	1K	2K	2K	2K	16K	16K	2K
Timer	•	•	•	•	•	•	•	•	•	•
Serial Port 0 (Multichannel)	•	•	—	•	•	•	•	•	•	•
Serial Port 1	•	•	•	•	•	•	•	•	•	•
Host Interface Port	—	—	—	—	•	•	•	—	—	•
DMA Ports	—	—	—	—	—	—	—	•	•	—
Analog Interface	—	—	—	—	—	—	—	—	—	•
Supply Voltage	5V	3.3V	5V	5V	5V	5V	3.3V	5V	3.3V	5V
Instruction Rate (MIPS)	20	10	13.8	20	20	33	20	33	33	26

Table 1.1 ADSP-2100 Family Processor Features & On-Chip Peripherals

- *Memory*—The ADSP-2100 family uses a modified Harvard architecture in which data memory stores data, and program memory stores both instructions and data. All ADSP-2100 family processors contain on-chip RAM that comprises a portion of the program memory space and data memory space. The speed of the on-chip memory allows the processor to fetch two operands (one from data memory and one from program memory) and an instruction (from program memory) in a single cycle.
- *Serial Ports*—The serial ports (SPORTs) provide a complete serial interface with hardware companding for data compression and expansion. Both μ -law and A-law companding are supported. The SPORTs interface easily and directly to a wide variety of popular serial devices. Each SPORT can generate a programmable internal clock or accept an external clock. SPORT0 includes a multichannel option.
- *Timer*—A programmable timer/counter with 8-bit prescaler provides periodic interrupt generation.
- *Host Interface Port*—The Host Interface Port (HIP) allows direct connection (with no glue logic) to a host processor. The HIP is made up of 16 data pins and 11 control pins. The HIP is extremely flexible and has provisions to allow simple interface to a variety of host processors. For example, the Motorola 68000, the Intel 8051, or another ADSP-2100 family processor can be easily connected to the HIP.