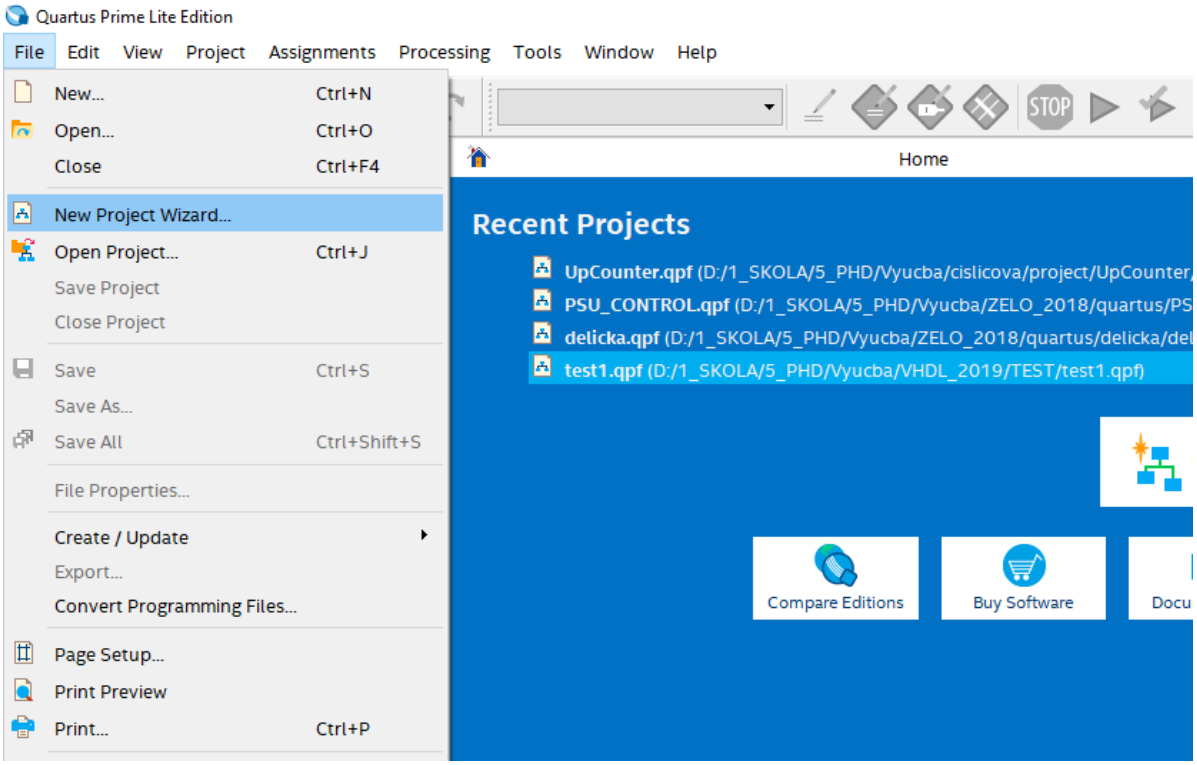
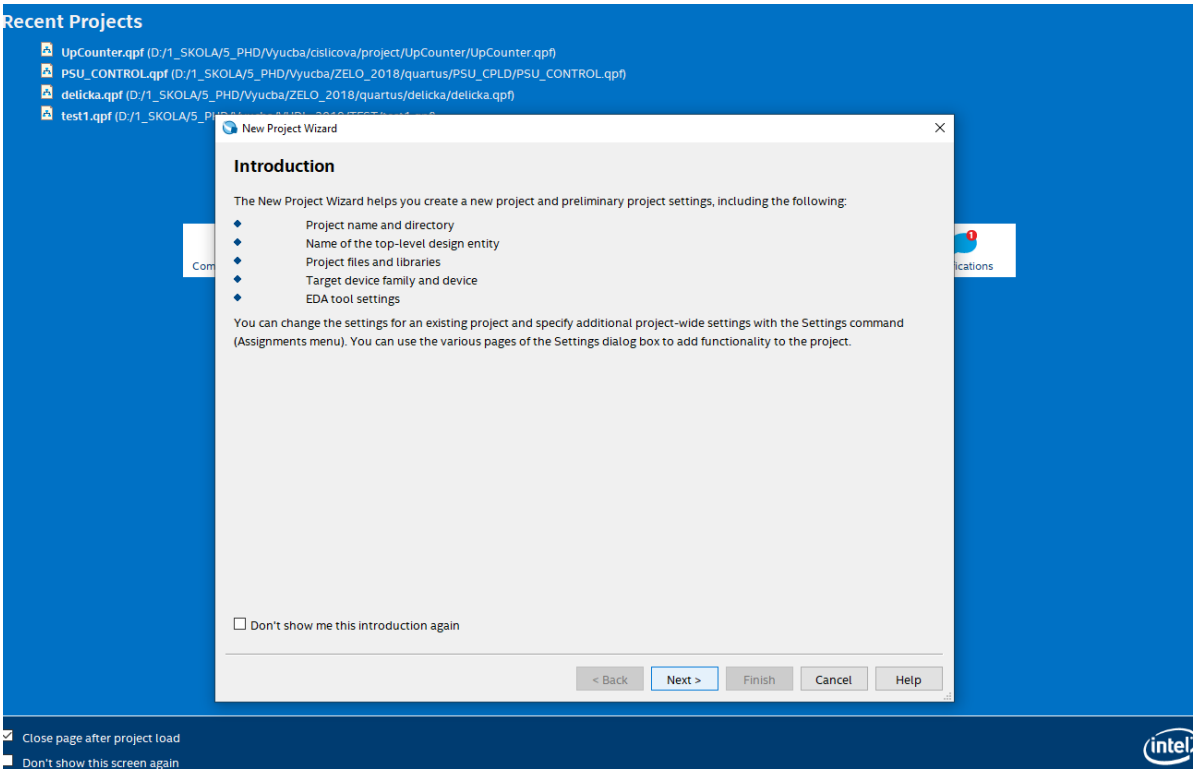
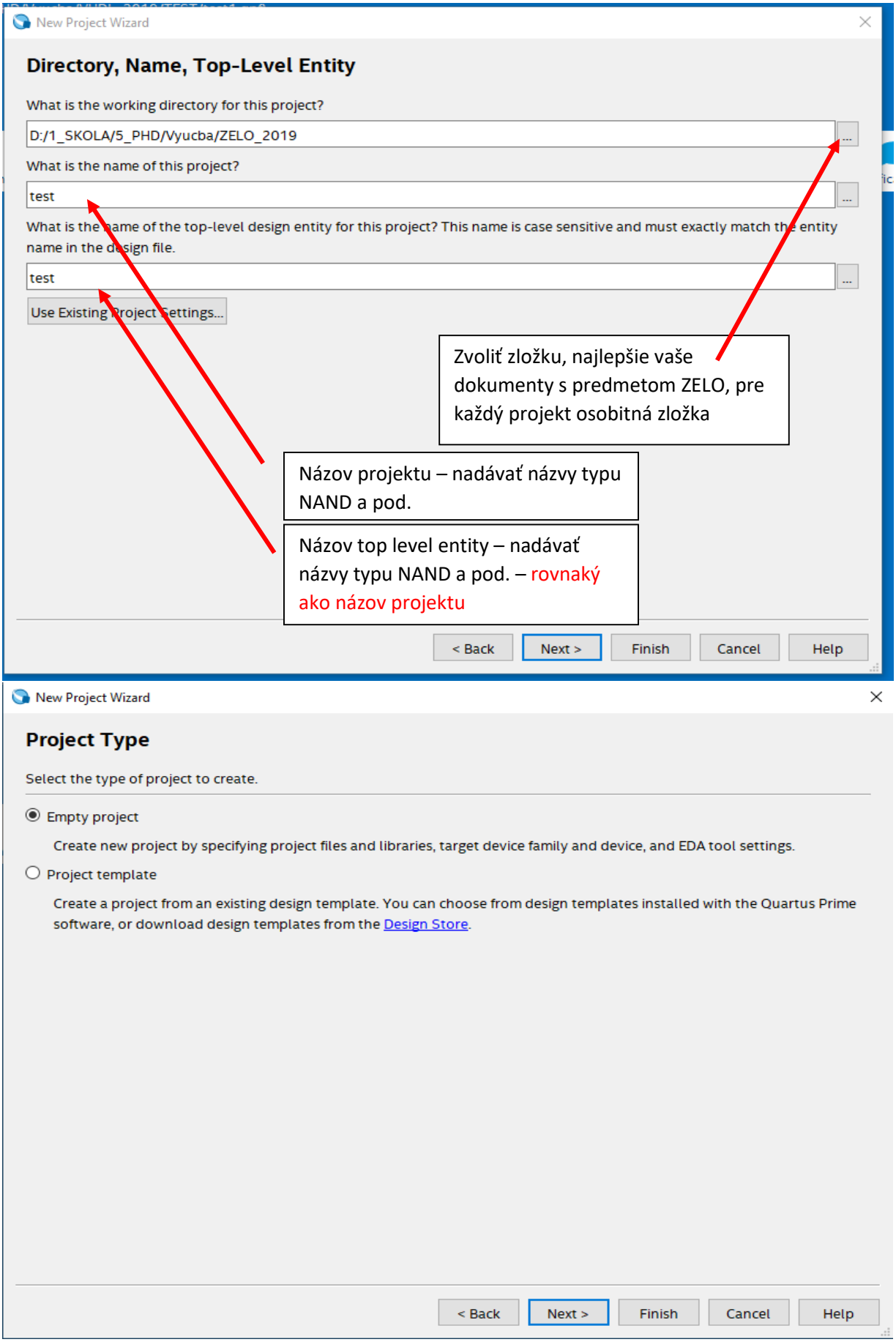
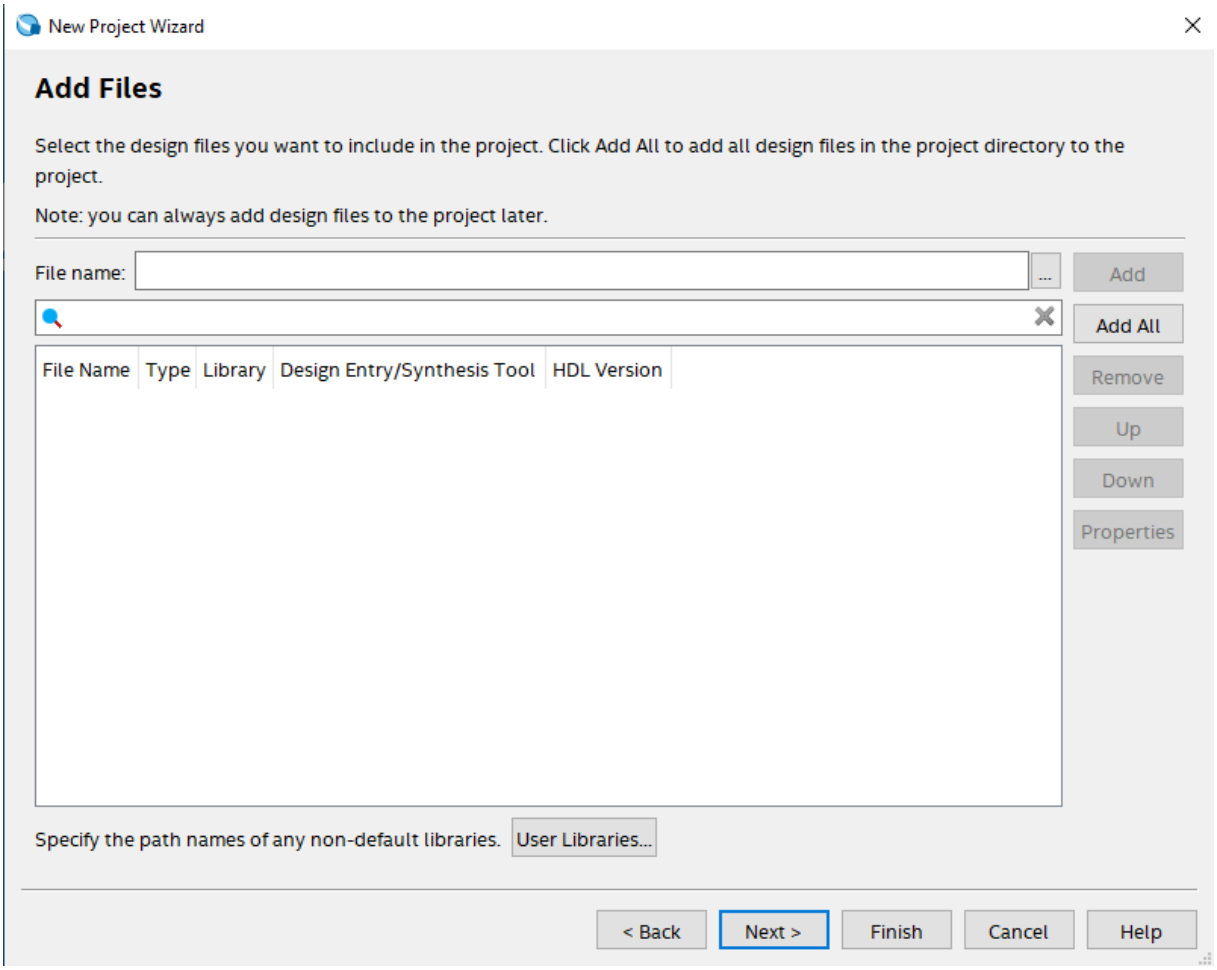
Quartus manuál

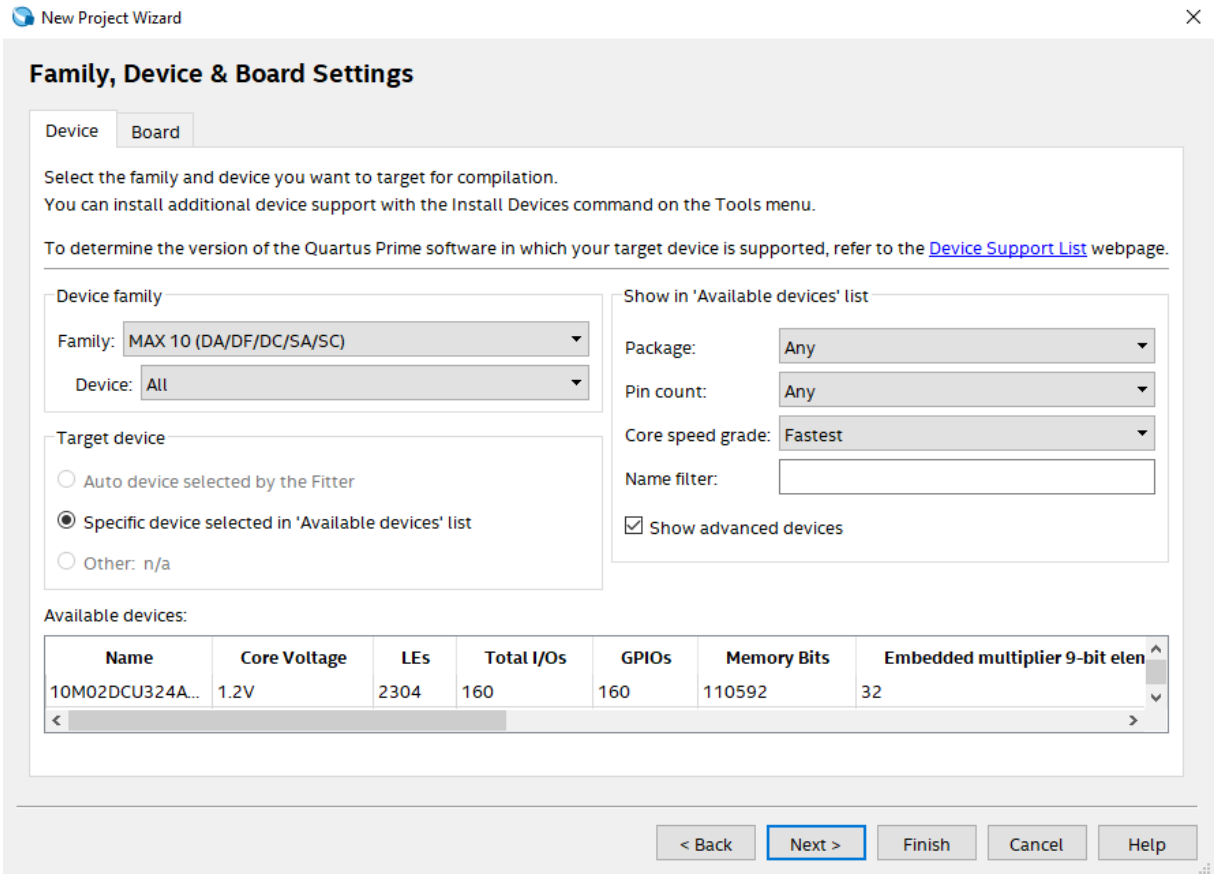
1. Vytvorenie projektu

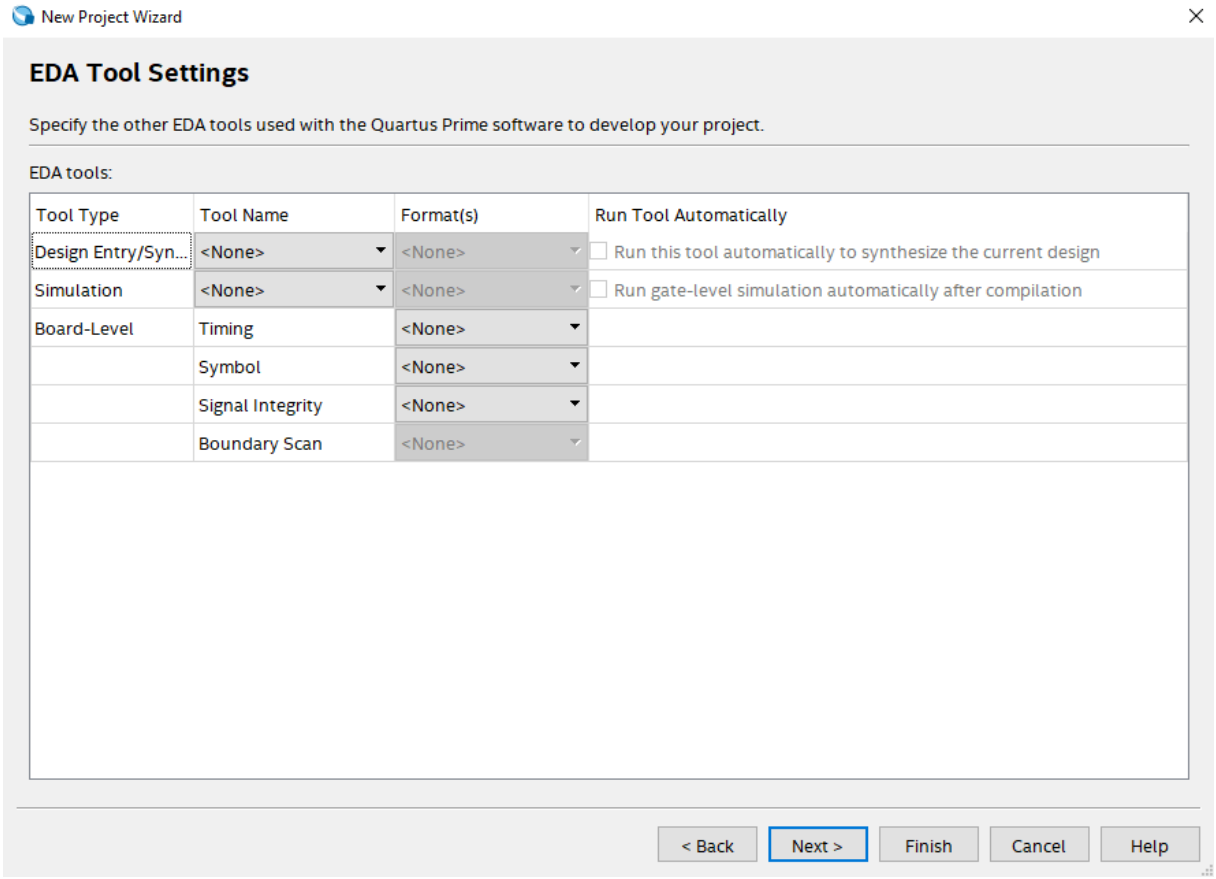


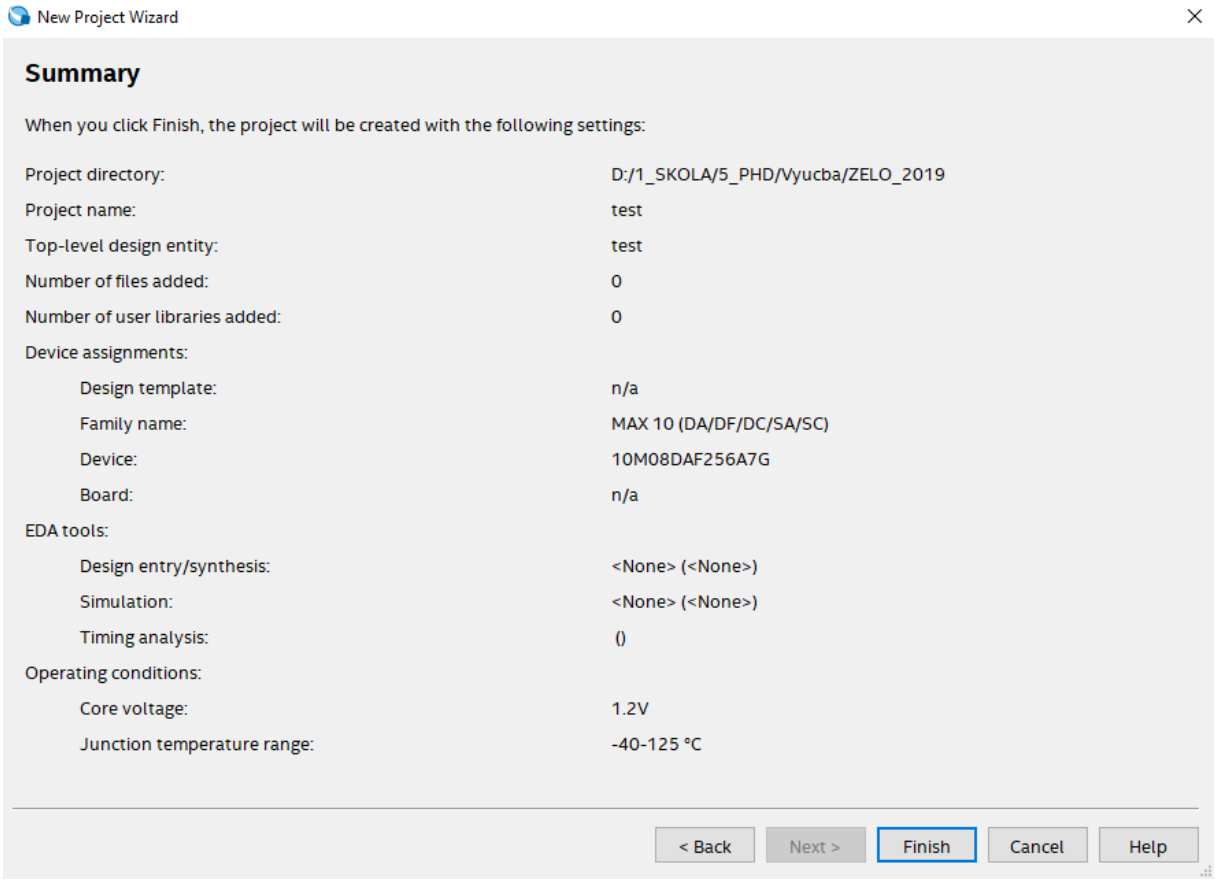


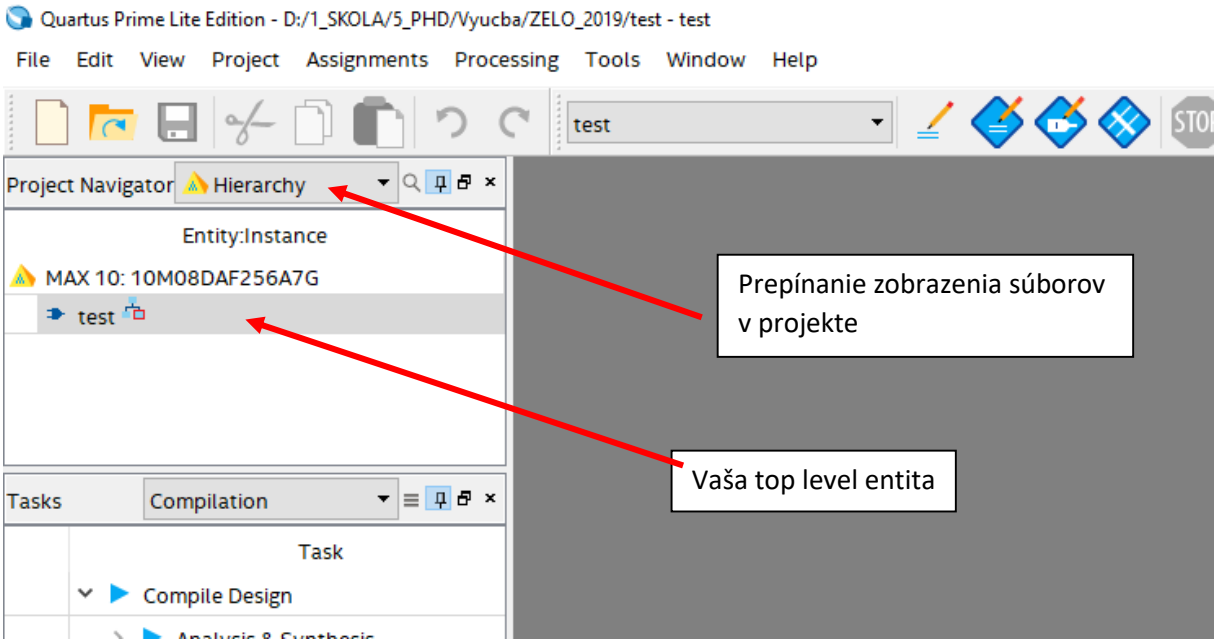

New Project Wizard
Directory, Name, Top-Level Entity
What is the working directory for this project?
D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019
What is the name of this project?
test
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
test
Use Existing Project Settings...
Zvoliť zložku, najlepšie vaše dokumenty s predmetom ZELO, pre každý projekt osobitná zložka
Názov projektu – nadávať názvy typu NAND a pod.
Názov top level entity – nadávať názvy typu NAND a pod. – rovnaký ako názov projektu
< Back
Next >
Finish
Cancel
Help
New Project Wizard
Project Type
Select the type of project to create.
Empty project
Create new project by specifying project files and libraries, target device family and device, and EDA tool settings.
Project template
Create a project from an existing design template. You can choose from design templates installed with the Quartus Prime software, or download design templates from the Design Store.
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Add Files
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Specify the path names of any non-default libraries.
User Libraries...
< Back
Next >
Finish
Cancel
Help

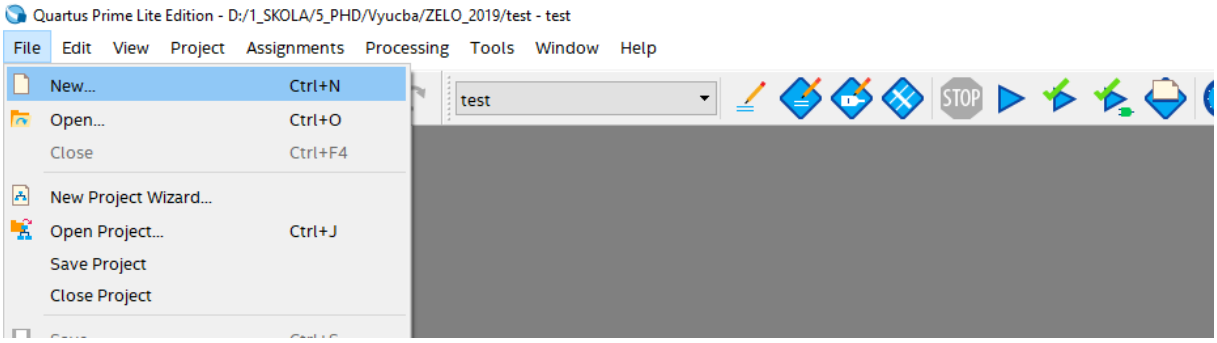

New Project Wizard
Family, Device & Board Settings
Device
Board
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported, refer to the Device Support List webpage.
Device family
Family: MAX 10 (DA/DF/DC/SA/SC)
Device: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Core speed grade: Fastest
Name filter:
Show advanced devices
Available devices:
Name
Core Voltage
LEs
Total I/Os
GPIOs
Memory Bits
Embedded multiplier 9-bit elen
10M02DCU324A...
1.2V
2304
160
160
110592
32
< Back
Next >
Finish
Cancel
Help

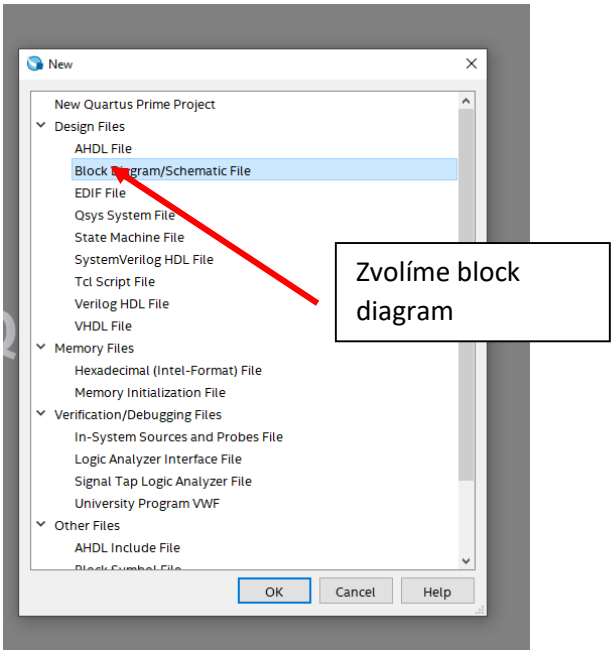

New Project Wizard
EDA Tool Settings
Specify the other EDA tools used with the Quartus Prime software to develop your project.
EDA tools:
Tool Type
Tool Name
Format(s)
Run Tool Automatically
Design Entry/Syn...
<None>
<None>
Run this tool automatically to synthesize the current design
Simulation
<None>
<None>
Run gate-level simulation automatically after compilation
Board-Level
Timing
<None>
Symbol
<None>
Signal Integrity
<None>
Boundary Scan
<None>
< Back
Next >
Finish
Cancel
Help

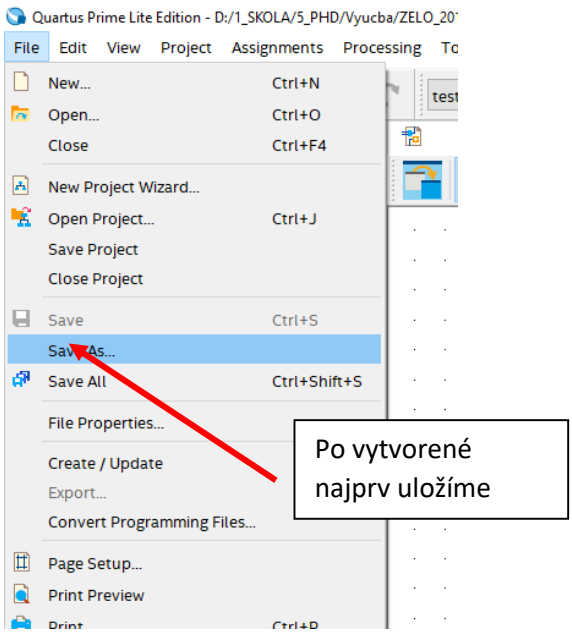

New Project Wizard
Summary
When you click Finish, the project will be created with the following settings:
Project directory:
D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019
Project name:
test
Top-level design entity:
test
Number of files added:
0
Number of user libraries added:
0
Device assignments:
Design template:
n/a
Family name:
MAX 10 (DA/DF/DC/SA/SC)
Device:
10M08DAF256A7G
Board:
n/a
EDA tools:
Design entry/synthesis:
<None> (<None>)
Simulation:
<None> (<None>)
Timing analysis:
()
Operating conditions:
Core voltage:
1.2V
Junction temperature range:
-40-125 °C
< Back
Next >
Finish
Cancel
Help

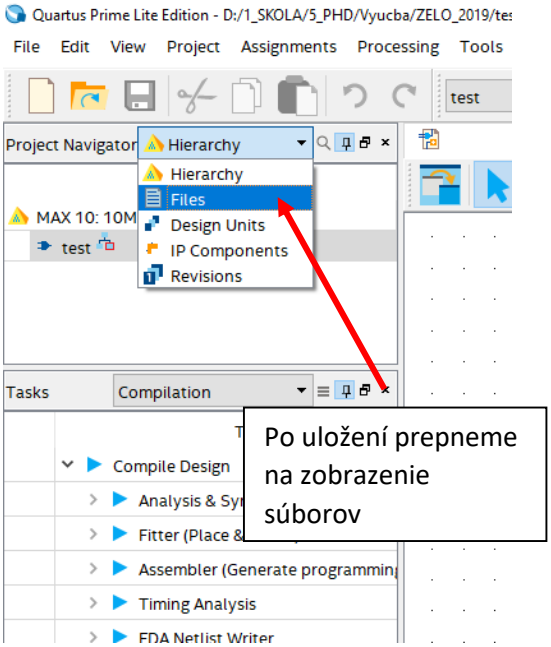


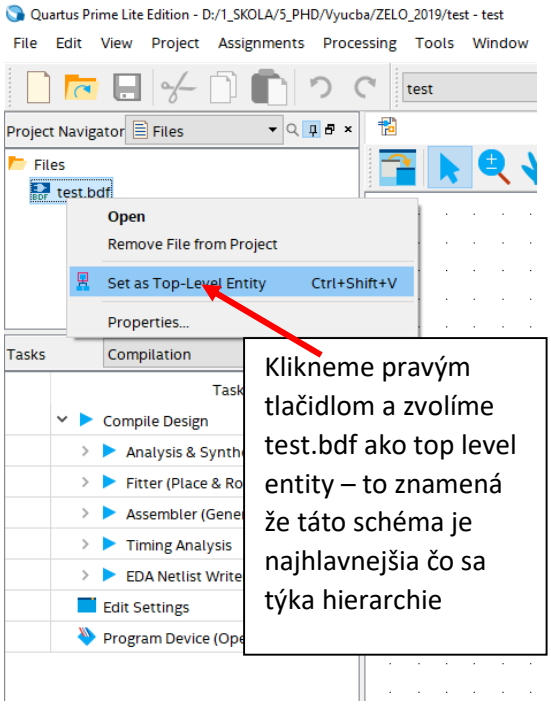
2. Vytvorenie schémy



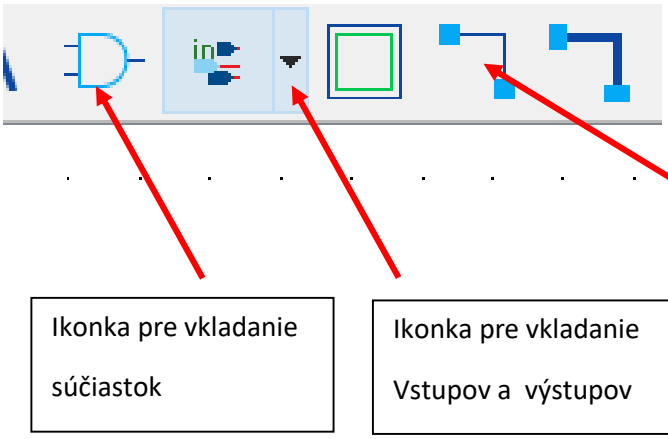

New
New Quartus Prime Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
Signal Tap Logic Analyzer File
University Program VWF
Other Files
AHDL Include File
OK
Cancel
Help
Zvolíme block diagram

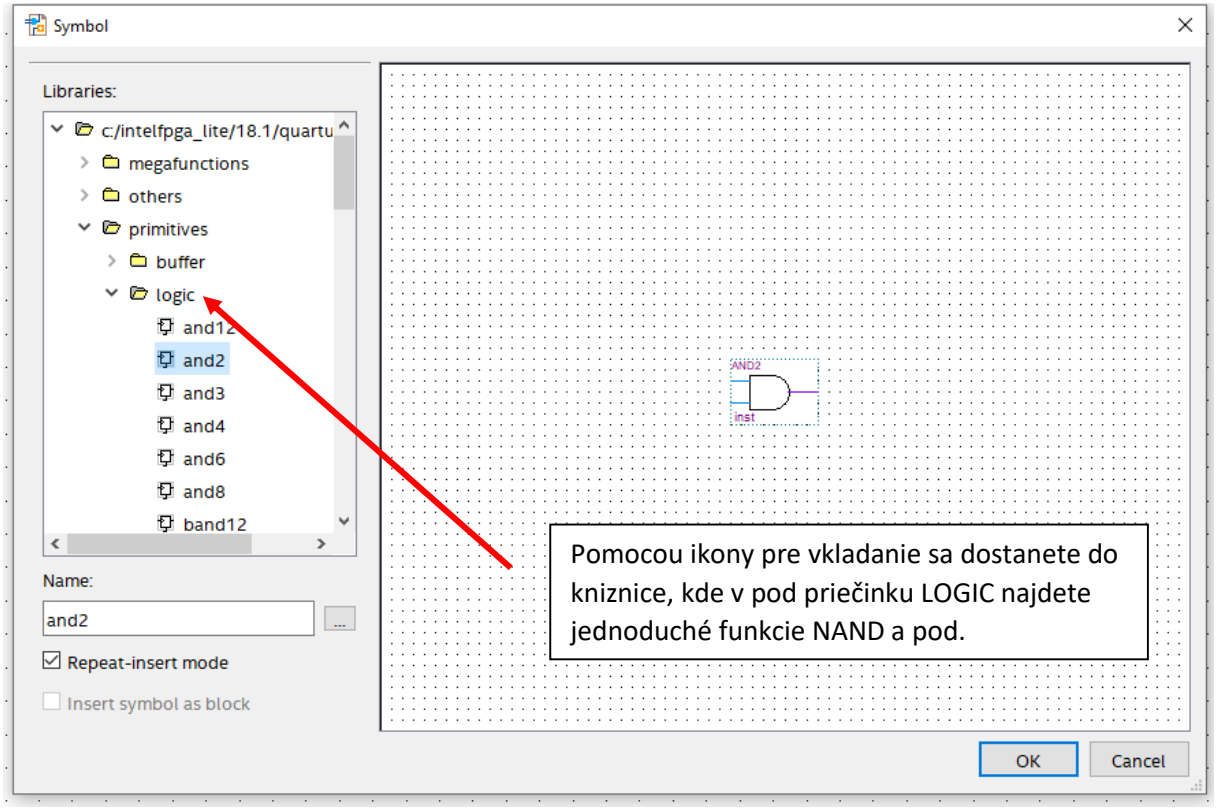

Quartus Prime Lite Edition - D:/1_SKOLA/5_PHD/Vyucba/ZELO_20
File
Edit
View
Project
Assignments
Processing
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Po vytvorené najprv uložíme

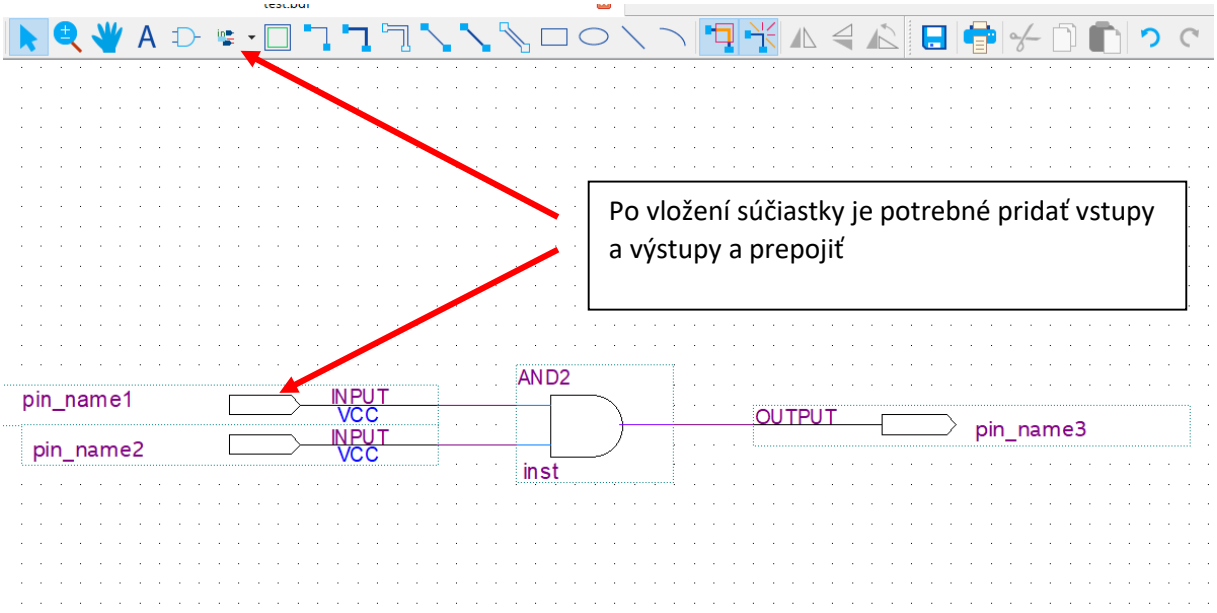

Quartus Prime Lite Edition - D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019/tes
File
Edit
View
Project
Assignments
Processing
Tools
test
Project Navigator
Hierarchy
Hierarchy
Files
Design Units
IP Components
Revisions
MAX 10: 10M
test
Tasks
Compilation
Compile Design
Analysis & Sy
Fitter (Place &
Assembler (Generate programmin
Timing Analysis
EDA Netlist Writer
Po uložení prepneme na zobrazenie súborov

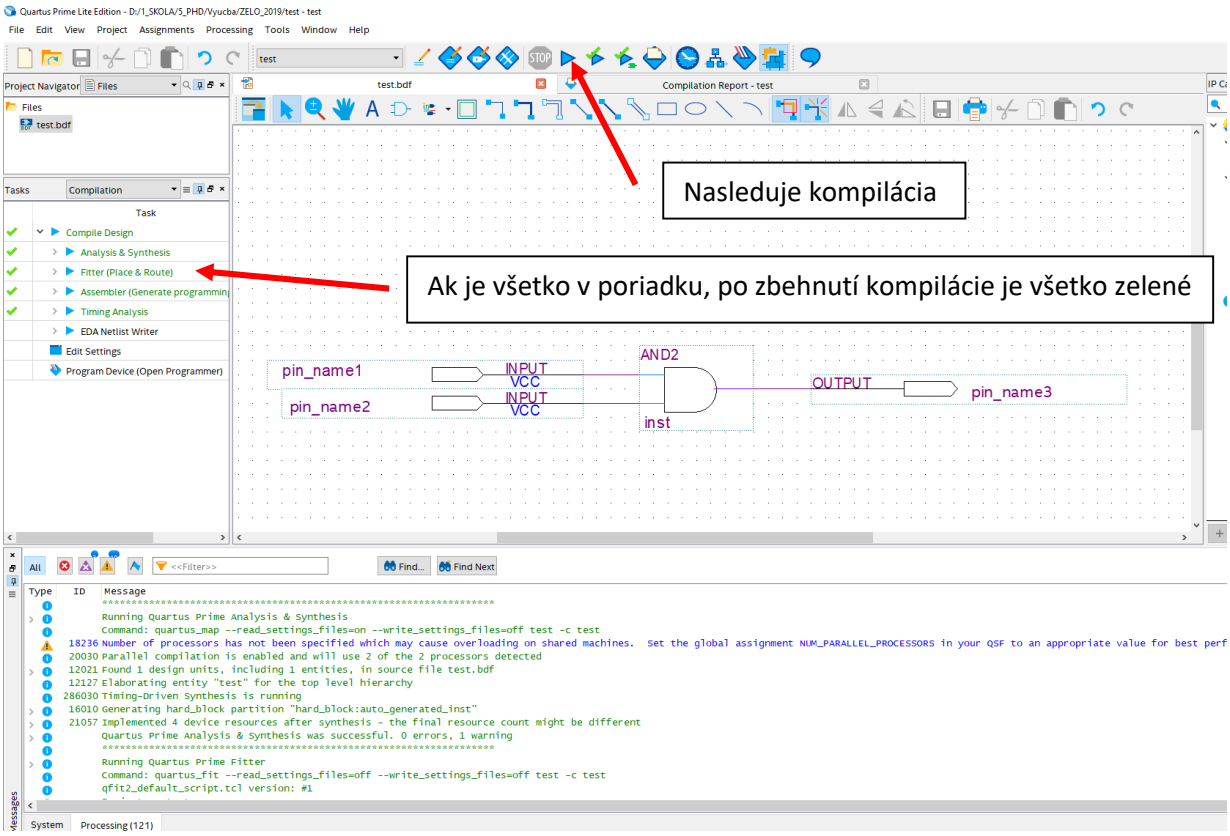

Quartus Prime Lite Edition - D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019/test - test
File
Edit
View
Project
Assignments
Processing
Tools
Window
test
Project Navigator
Files
Files
test.bdf
Open
Remove File from Project
Set as Top-Level Entity Ctrl+Shift+V
Properties...
Tasks
Compilation
Compile Design
Analysis & Synth
Fitter (Place & Ro
Assembler (Gene
Timing Analysis
EDA Netlist Write
Edit Settings
Program Device (Ope
Klikneme pravým tlačidlom a zvolíme test.bdf ako top level entity – to znamená že táto schéma je najhlavnejšia čo sa týka hierarchie

3. Vloženie prvkov do schémy

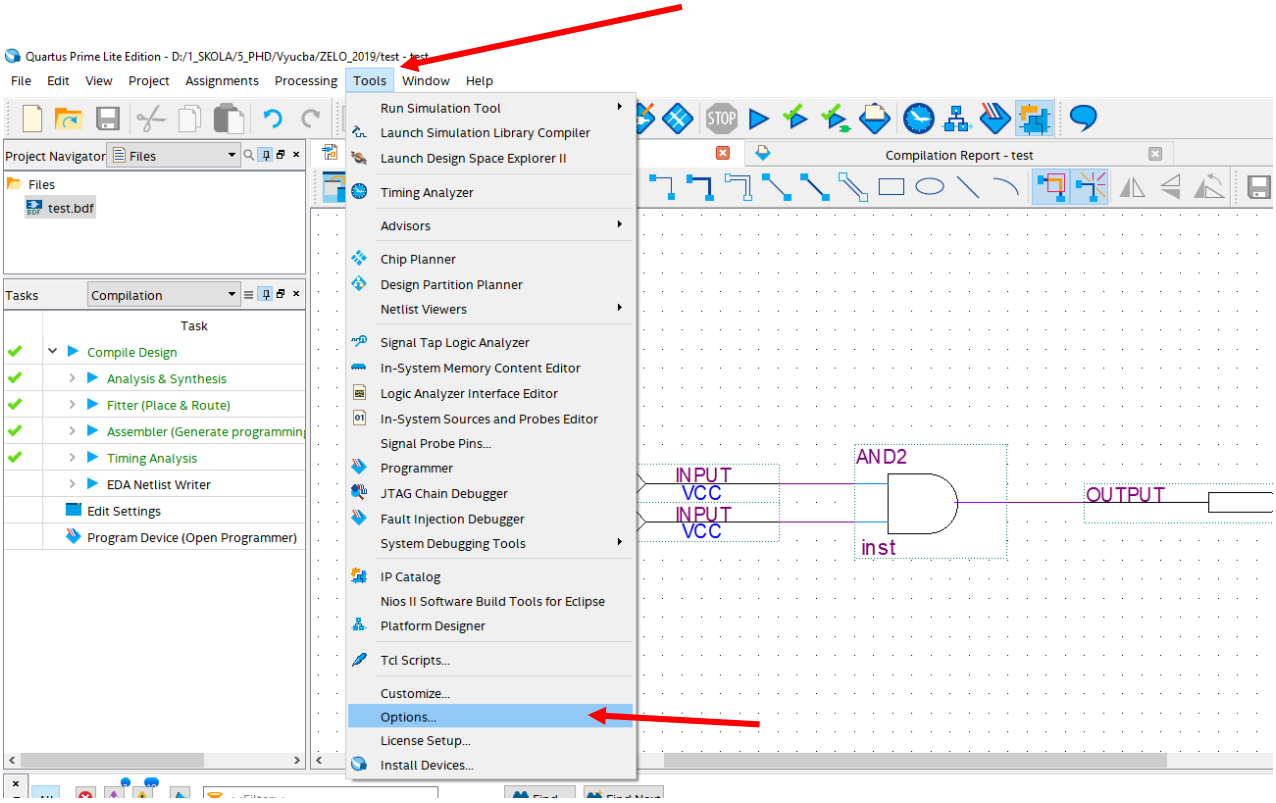


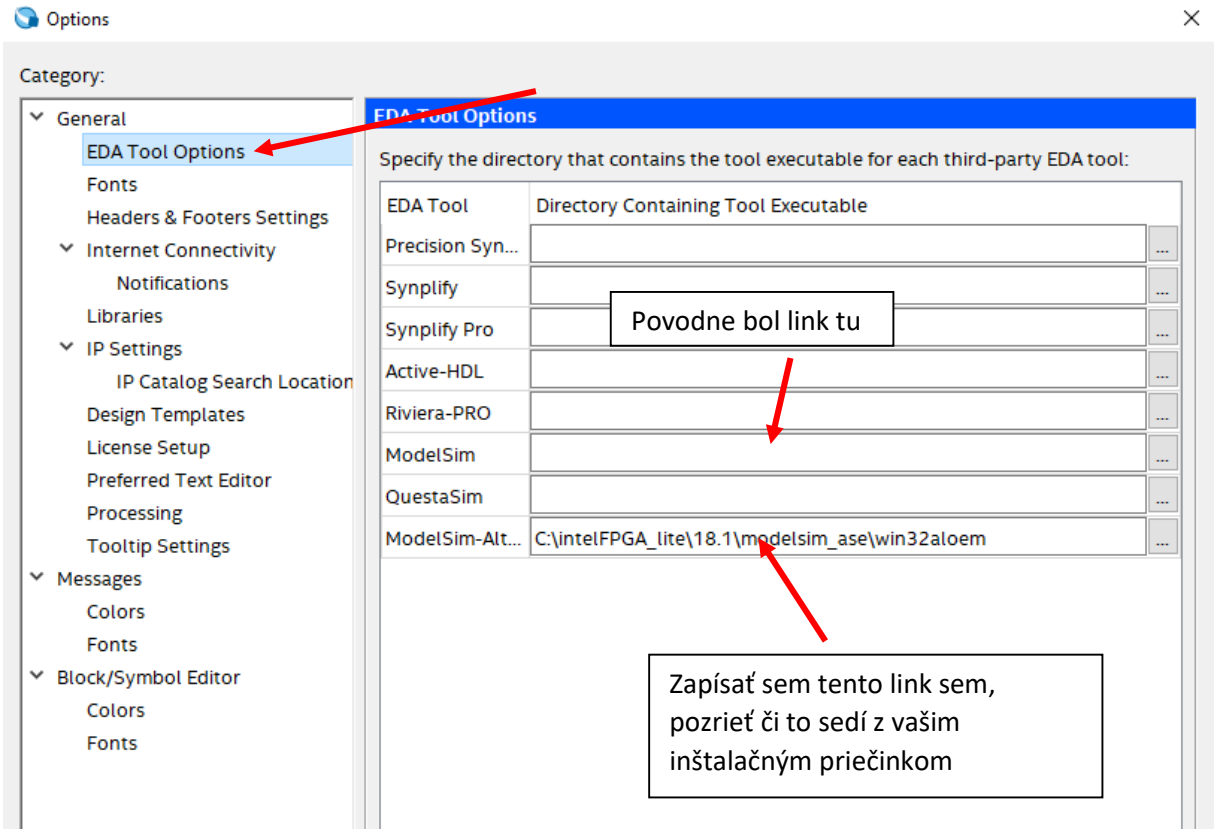



Po vložení súčiastky je potrebné pridať vstupy a výstupy a prepojiť
pin_name1
pin_name2
INPUT
VCC
INPUT
VCC
AND2
inst
OUTPUT
pin_name3

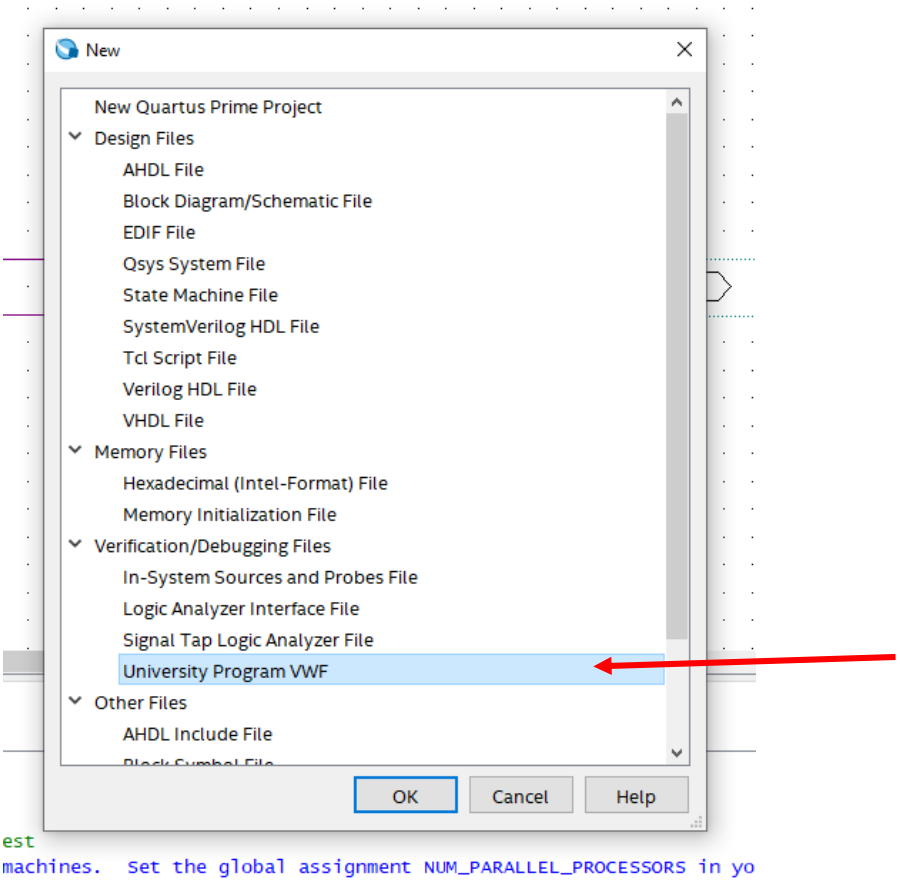

Nasleduje kompilácia
Ak je všetko v poriadku, po zbehnutí kompilácie je všetko zelené
pin_name1
pin_name2
INPUT
VCC
INPUT
VCC
AND2
inst
OUTPUT
pin_name3

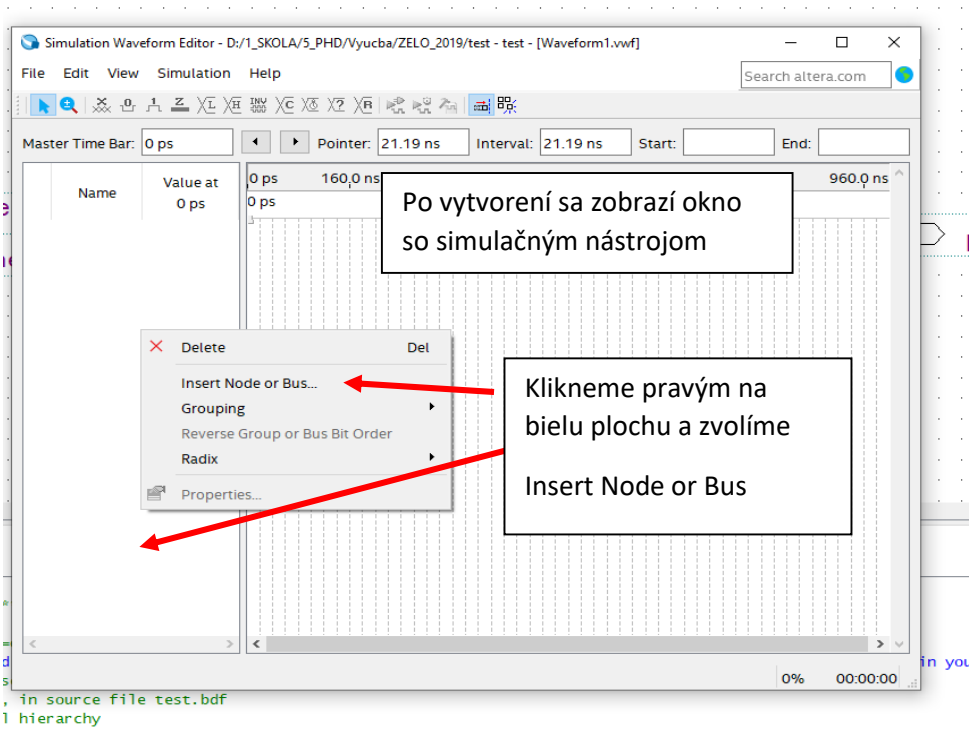
4. Nastavenie simulácie

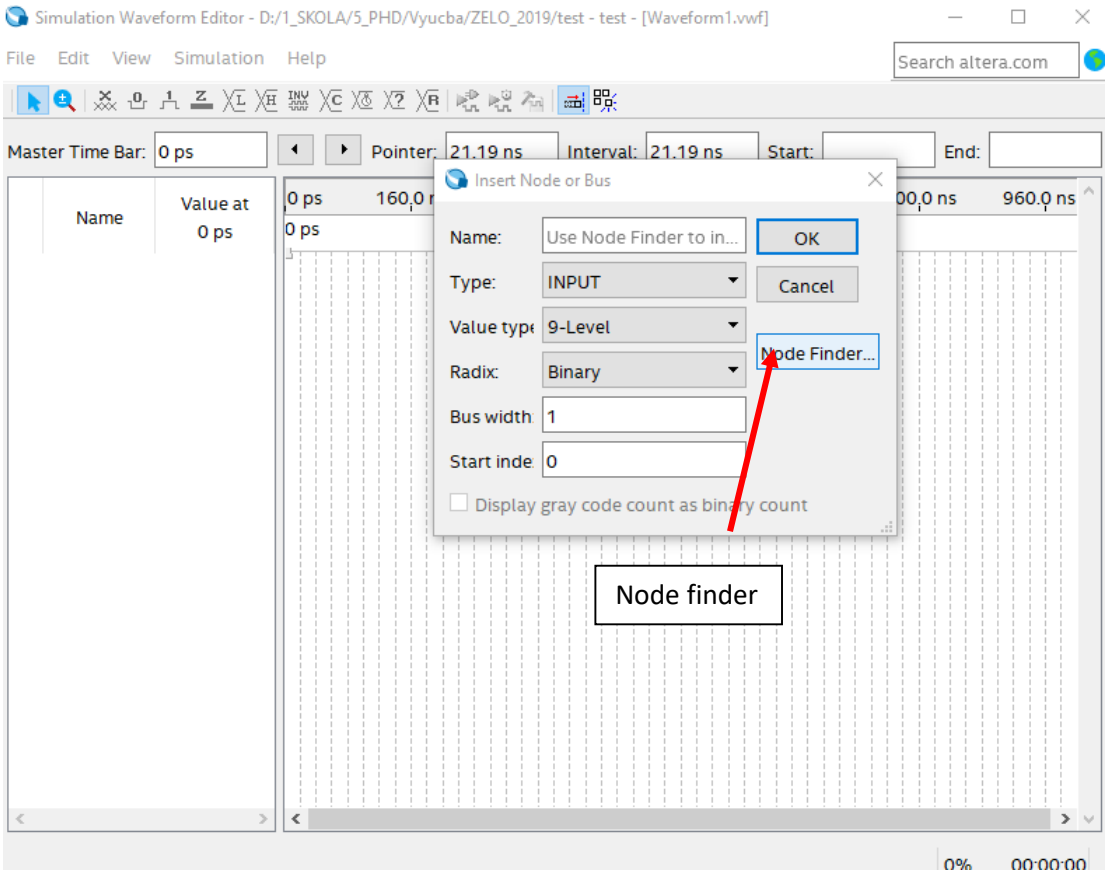


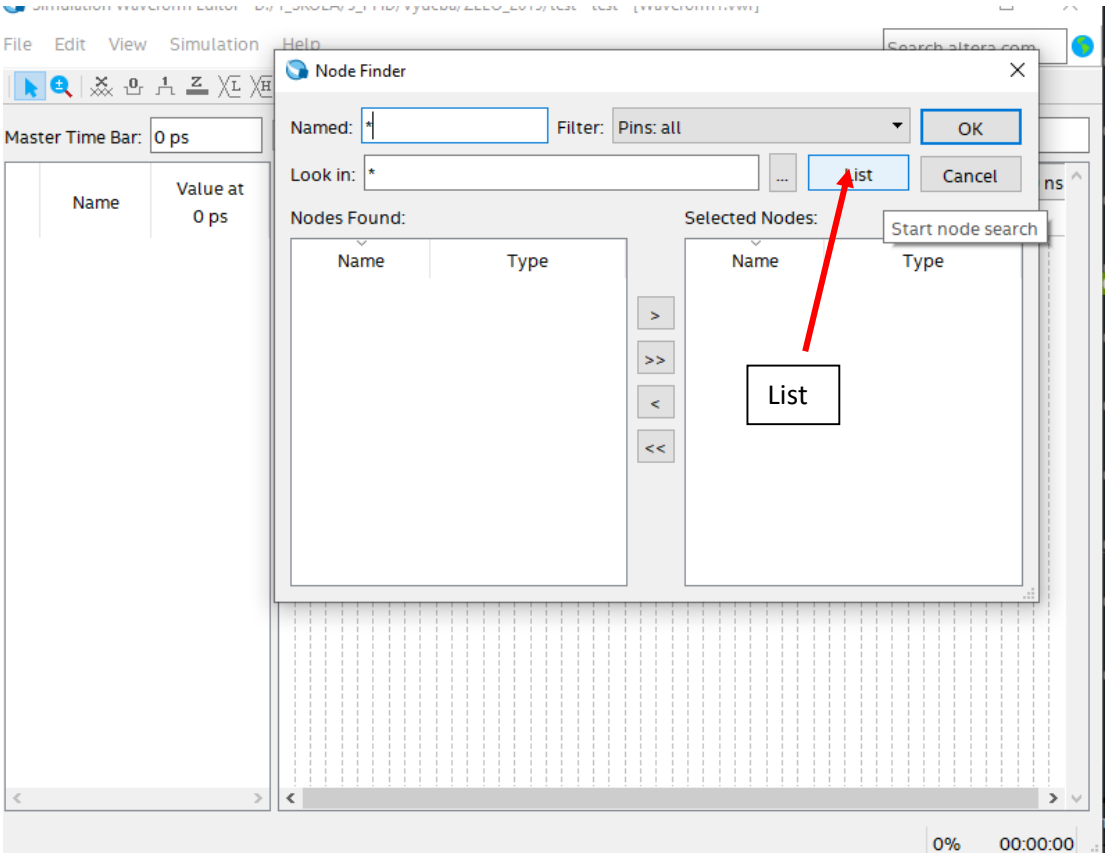


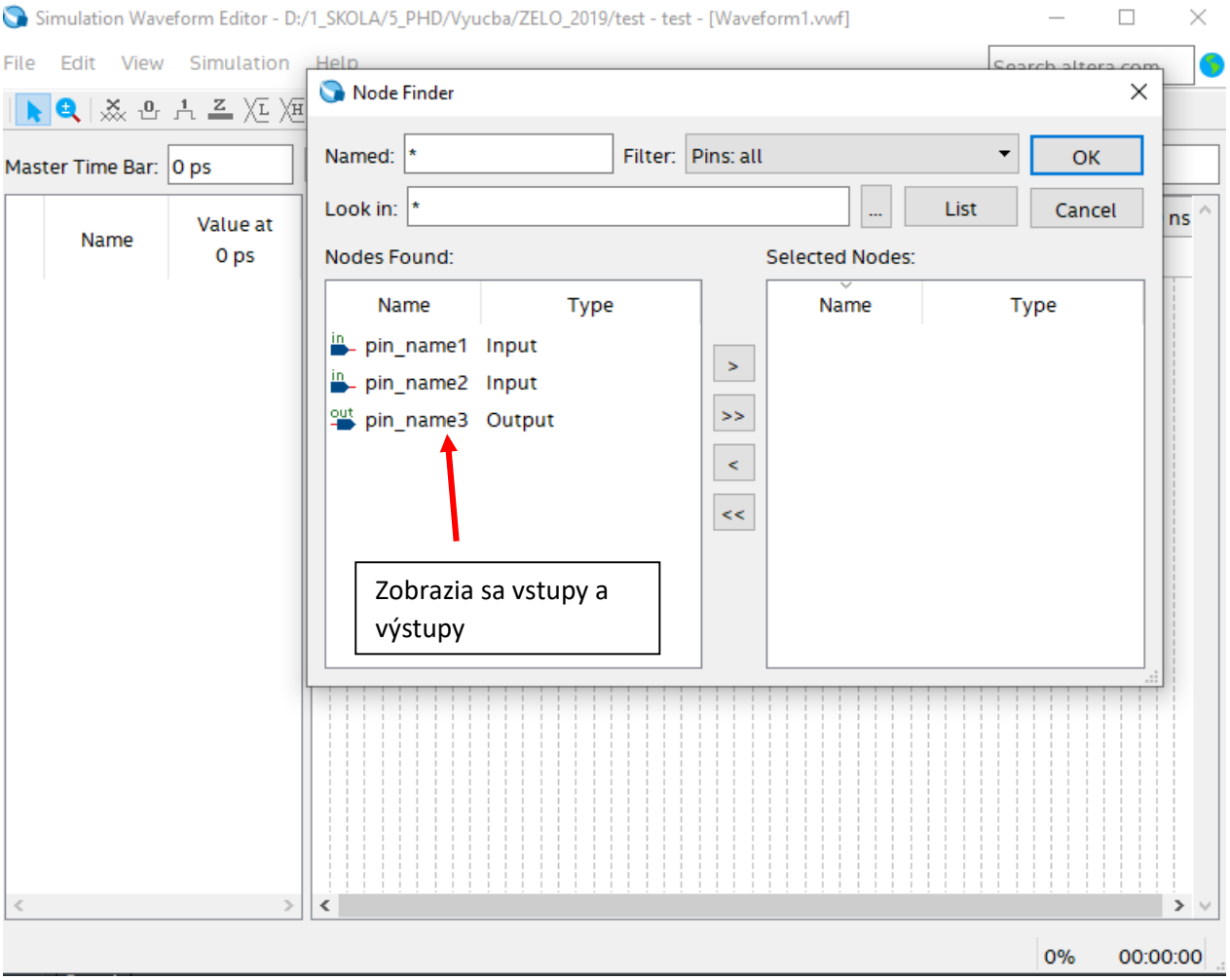
5. Vytvorenie simulácie

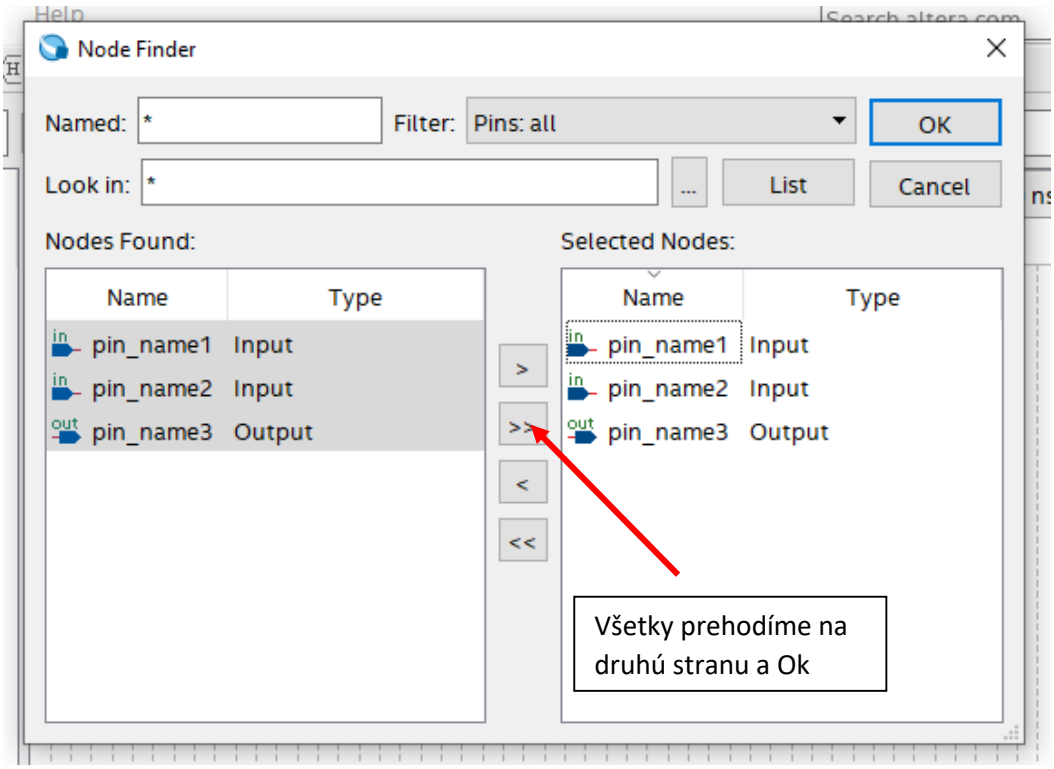


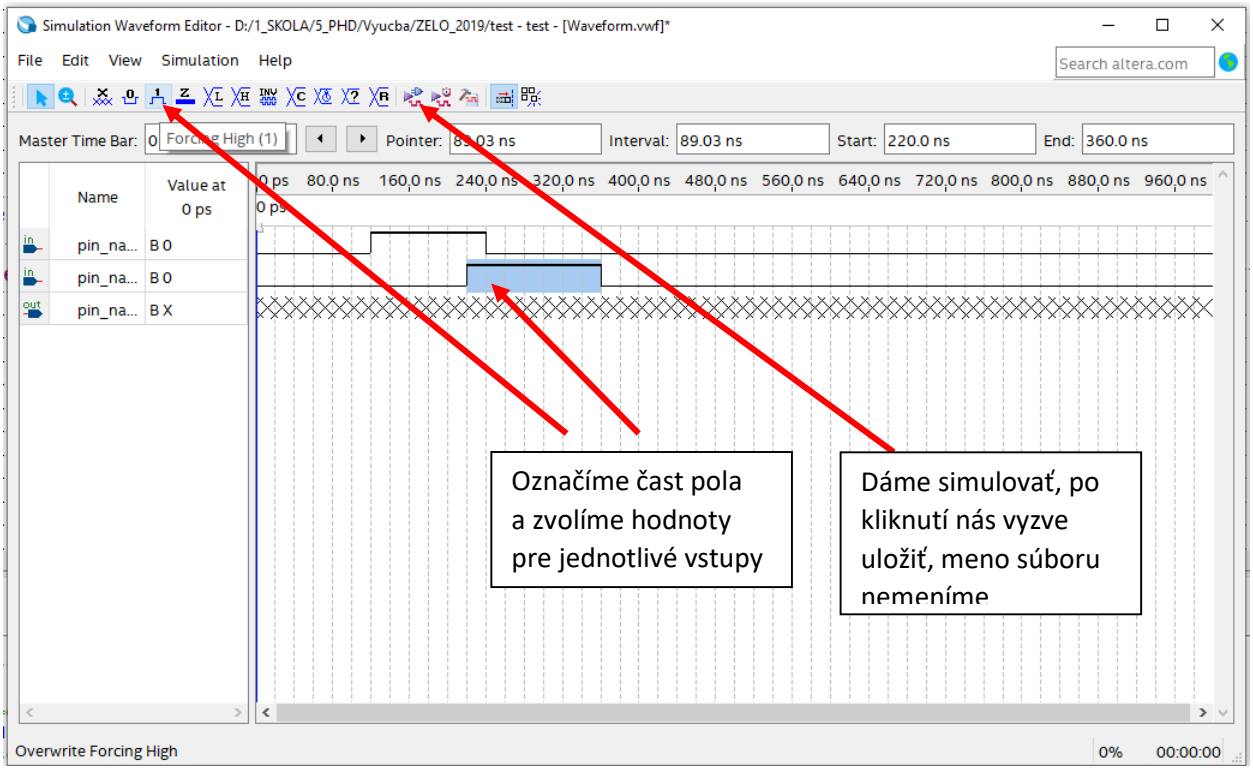


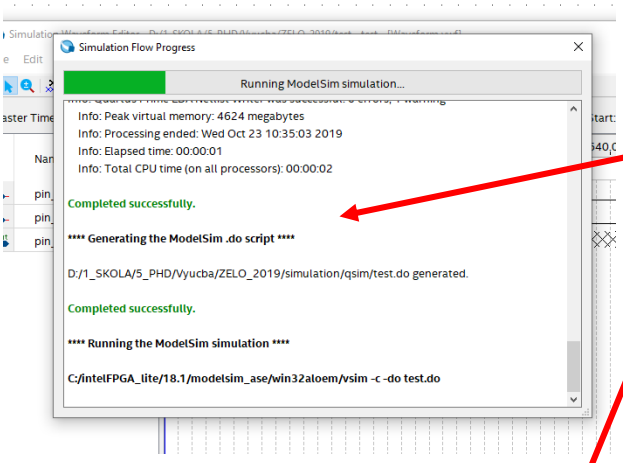

Simulation Waveform Editor - D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019/test - test - [Waveform1.vwf]
File Edit View Simulation Help
Search altera.com
Master Time Bar: 0 ps
Pointer: 21.19 ns
Interval: 21.19 ns
Start:
End:
Name
Value at 0 ps
Insert Node or Bus
Name: Use Node Finder to in...
OK
Type: INPUT
Cancel
Value type: 9-Level
Radix: Binary
Node Finder...
Bus width: 1
Start inde: 0
Display gray code count as binary count
Node finder
0%
00:00:00


File Edit View Simulation Help
Master Time Bar: 0 ps
Name
Value at 0 ps
Node Finder
Named: *
Filter: Pins: all
OK
Look in: *
List
Cancel
Start node search
Nodes Found:
Name
Type
Selected Nodes:
Name
Type
List
0%
00:00:00


Simulation Waveform Editor - D:/1_SKOLA/5_PHD/Vyucba/ZELO_2019/test - test - [Waveform1.vwf]
File Edit View Simulation Help
Master Time Bar: 0 ps
Name
Value at 0 ps
Node Finder
Named: *
Filter: Pins: all
OK
Look in: *
List
Cancel
Nodes Found:
Selected Nodes:
Name Type
pin_name1 Input
pin_name2 Input
pin_name3 Output
Zobrazia sa vstupy a výstupy
0%
00:00:00


Node Finder
Named: *
Filter: Pins: all
OK
Look in: *
List
Cancel
Nodes Found:
Selected Nodes:
Name Type
pin_name1 Input
pin_name2 Input
pin_name3 Output
Všetky prehodíme na druhú stranu a Ok





Priebeh simulácie a výsledok